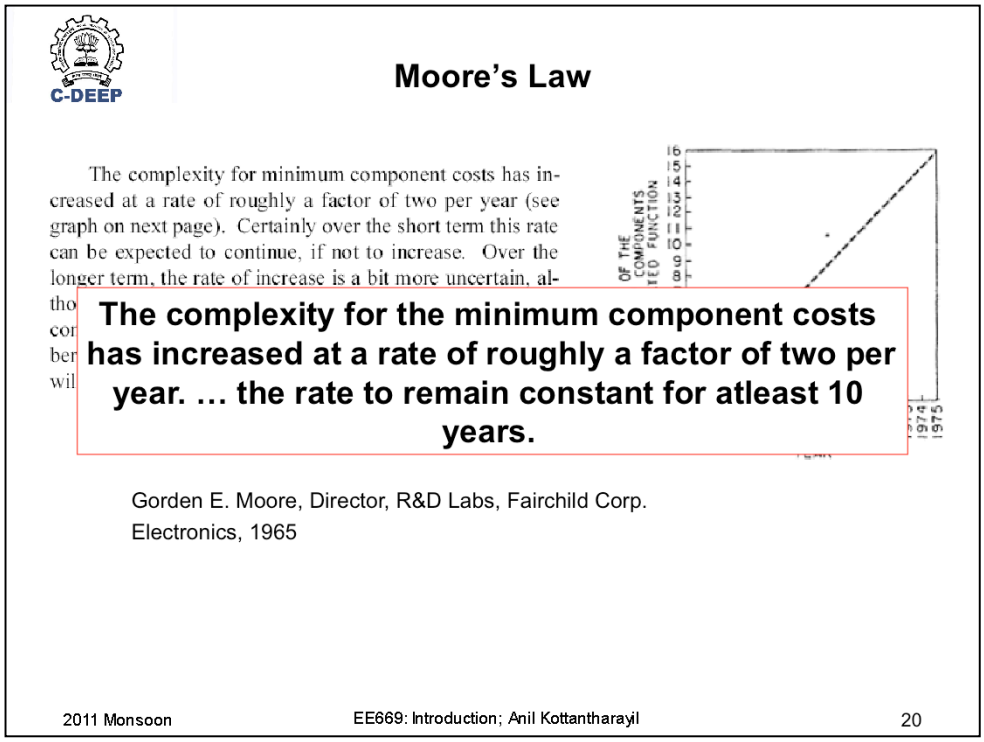

So far we discussed mostly technical aspects of VLSI technology. However development and application of technology is also an important economic activity. An important observation made by Gorden Moore, who along with Robert Noyce and others started Intel was that the the complex circuit with the minimum component cost increases roughly a factor of two every year. He predicted that this would continue for several years. This prediction was made in 1965.

This is pretty much like a stock market analyst's prediction. However the observation has proved to be the holy trail for the semiconductor industry.

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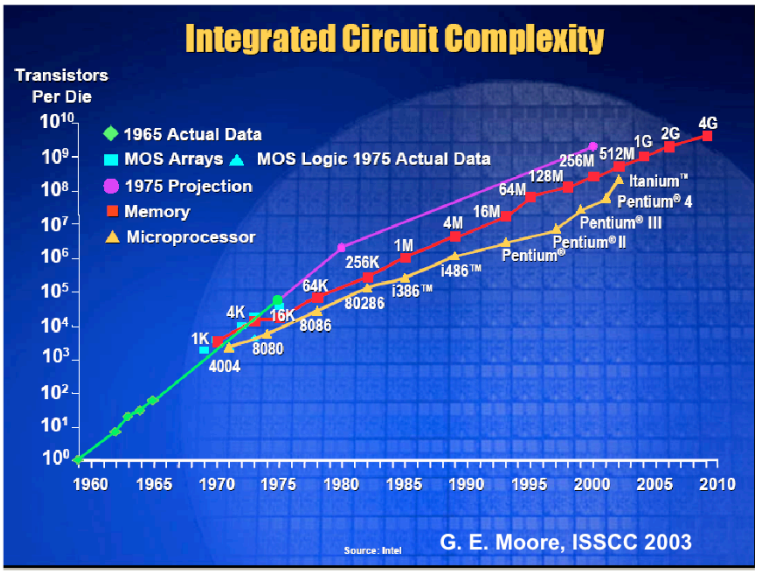
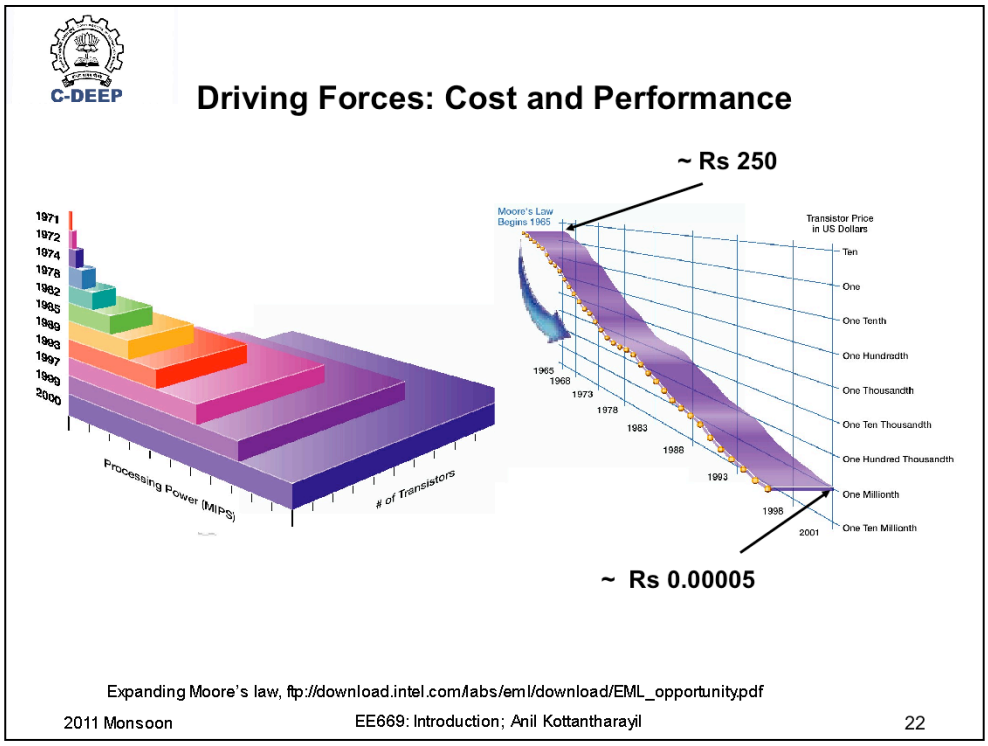
VLSI era



The semiconductor industry has taken the prophecy of Gorden Moore seriously as you can see on this slide. This slide shows the number of transistors per chip for various categories of integrated circuits. You can see that the number of transistors per chip has increased from about 10 in early 1960's to several billions by 2010. 8 orders of magnitude increase.

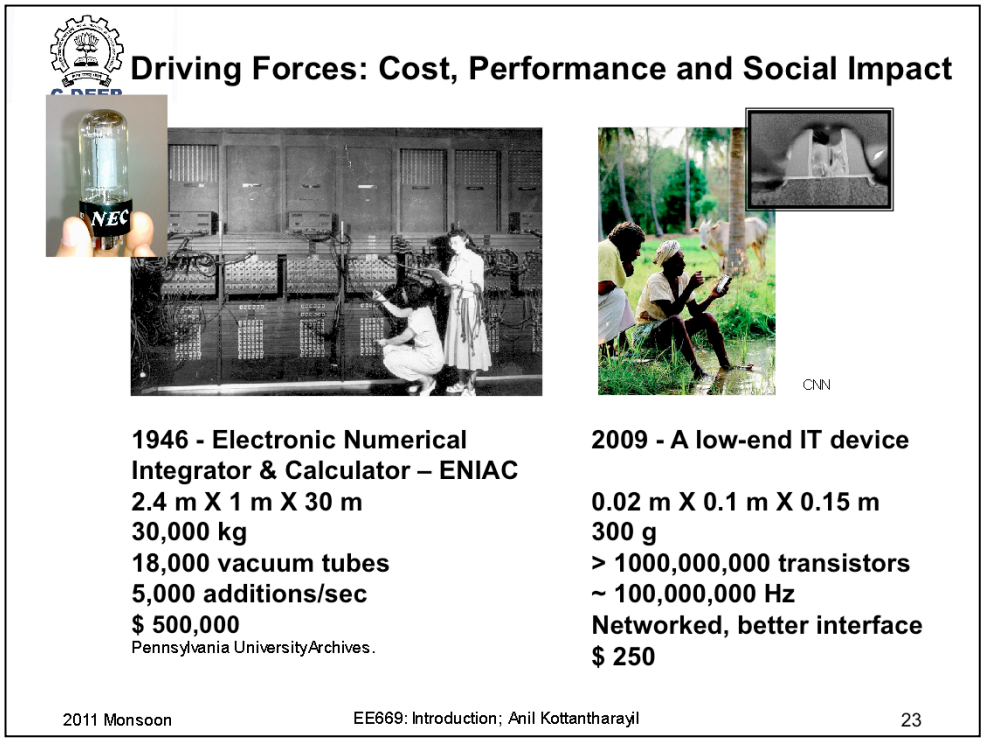


What are the motivations for this dramatic increase in integration density.

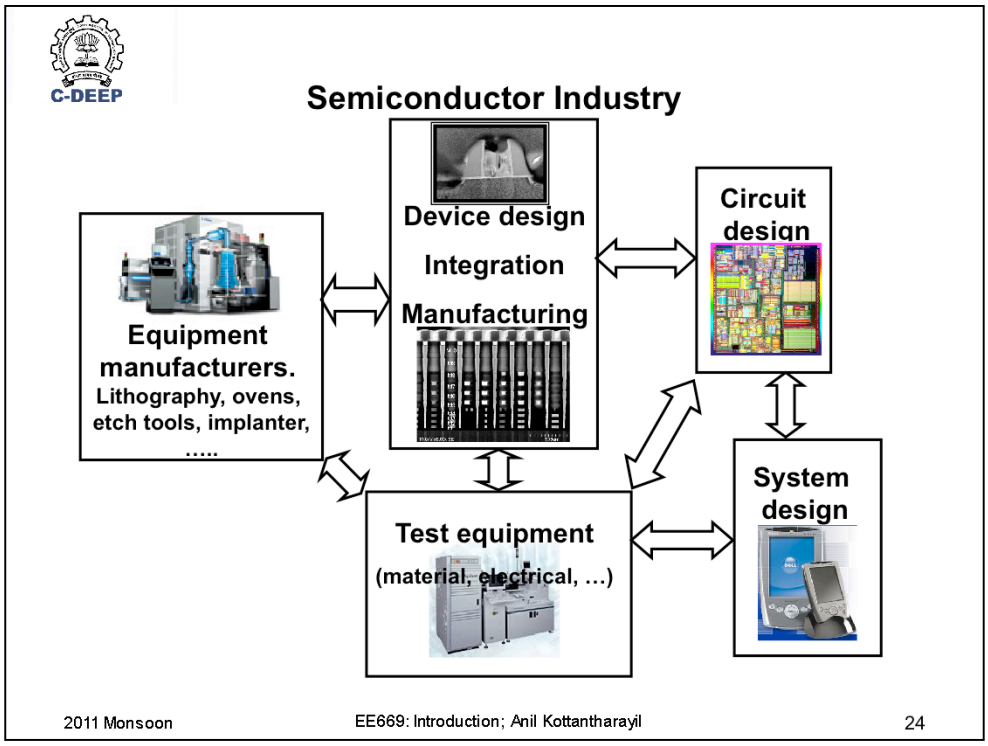
More complex circuits can be integrated on a single chip. So we have a whole mobile communication system on a chip and there are several such examples. It is increasingly viable to integrate whole electronic systems on a single chip.

The speed of devices have increased. The figure shows that every year the instruction processing rate of microprocessors have increased many fold since the early microporcessor. So the performance increase is a very important motivation.

The cost has decreased dramatically. We had seen earlier that the early transistors were as expensive as 150 dollars. In today's cost i.e. 1000 $ ~ Rs 45000. By 2001 that has fallen to 0.00005 Rs. This has also made complex electronic systems affordable to large number of people with a significant improvement in the quality of life. In the early stages of transistor electronics, military and space were the main users of electronic equipment. These are linked to protection of nation states and their pride and no one counted the money spent on these.



1. ENIAC made at the University of Pennsylvania in 1946 by John Mauchly and Presper Eckert for US army ordnance. Used in second world war for calculation of missile projectile tables.
2. It was thought of as the first electronic computer till 1973.
3. This fascinating success story in engineering, which had a decisive impact on the way we live also has a fascinating science and technology behind it. This is represented by the devices within these contrasting systems.
4. The left hand side shows the picture of a vacuum tube. 18000 of them were inside one of those early machines. You could hold 10 of them in your palm. The transistor based systems, the whole of it, can be held in your hand.



The complexity of the electronics industry also grew with complex circuits. This slide shows a snapshot of various sub – industries of the electronic system market and the interplay between them. We will learn how VLSI circuits are fabricated. However you need equipment for manufacturing the circuits, you need a design of the circuit, you need tools for designing circuits, what ever you manufacturer should be tested to specification, an so on. It is not possible for monolithic companies to manage such divergent activities. However the activities must be coordinated for the whole industry to work. For example, a IC manufacturing company decide to come to the market with ICs containing 10nm wide features. The company must have equipment to produce this, equipment to measure such features and also a market where such Ics would find applications. So doing it alone would not help. One of the reason is the cost involved.

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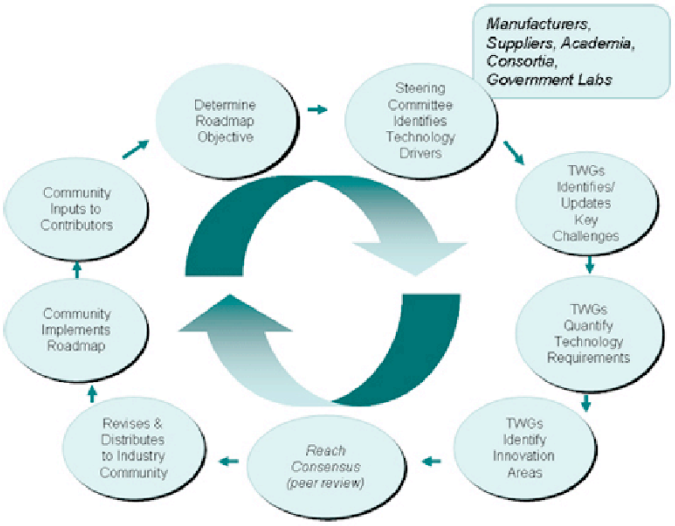
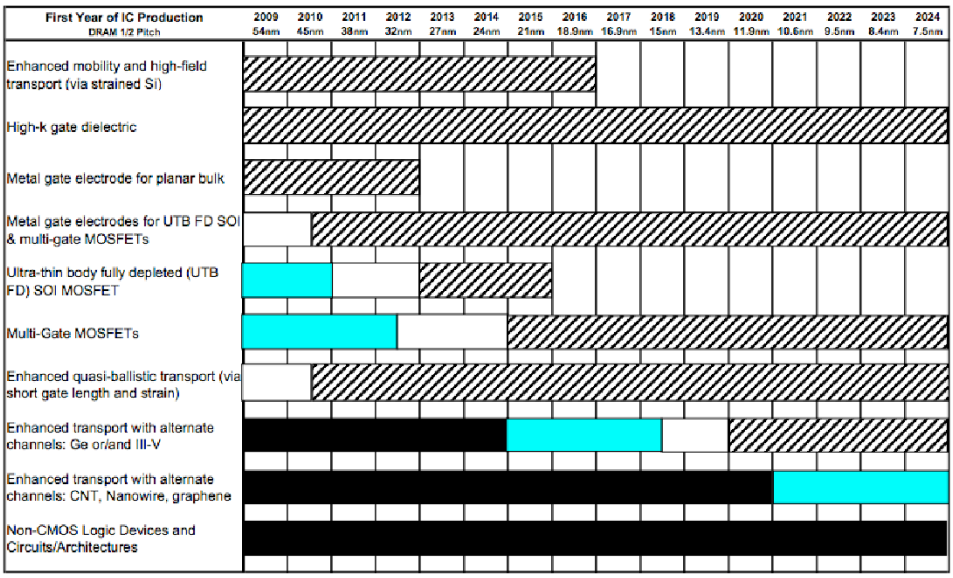
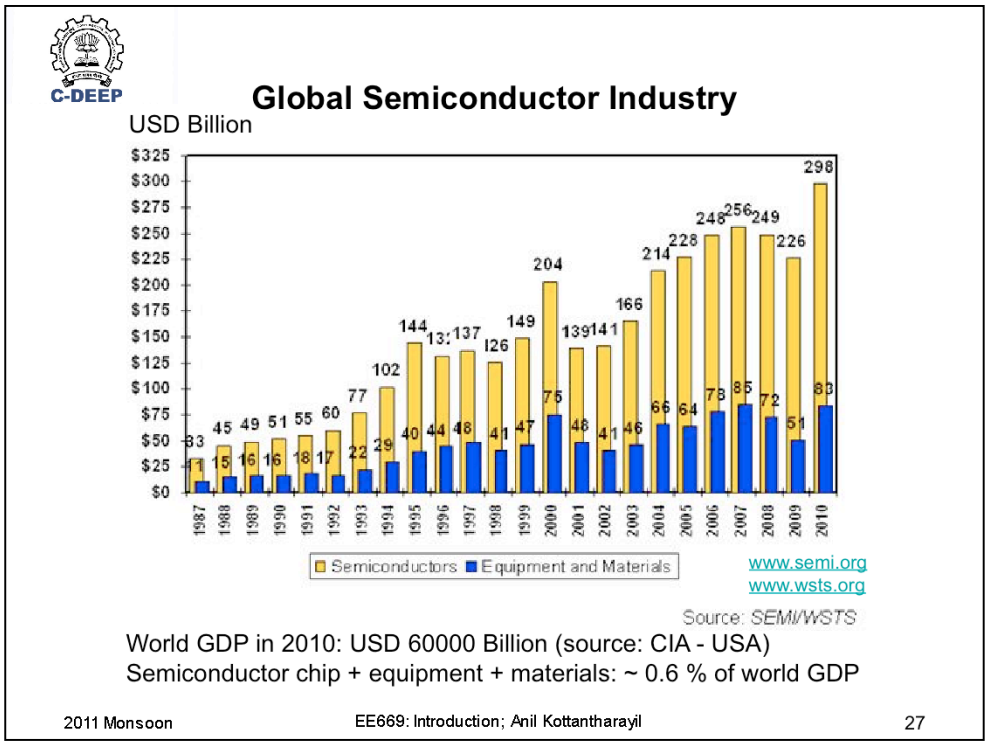
International Technology Roadmap for Semiconductors (ITRS)



www.itrs.net



ITRS 2009 edition
Process Integration, devices, and structures



This slide shows the global semiconductor industry revenues since 1987. The semiconductor industry contributes 0.6 % of the world's GDP. In india, that is less than 0.01%. On the other hand the recent estimates suggests that by 2020 our electronic component import would exceed our oil bill. A very unsustainable scenario.

WSTS: World semiconductor trade statistics

SEMI:

Centre of Excellence in Nanoelectronics

- Started in 2006 as a 5-year joint project at IIT-B and IISc funded by DIT. Total funding of Rs 100 crore from DIT.
- IIT-B to focus on device oriented work
- Applied Materials Inc. (AMAT) donated equipment worth about Rs. 41 crore to IITB
- IITB internal funding of Rs. 20 crore
- Laboratory space of 15000 sq. ft., plus a new building of 20000 sq. ft. to be completed by June 2011
- 25 faculty members and 120 post-graduate students from various departments of IIT-B use the CEN facilities
- Additional investment of ~ 115 crores in the pipeline (ISRO, DRDO, DIT, …..)

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Examples of Equipment in CEN

Plasma Implanter

Double Sided Aligner

E B Evaporation

Furnaces

20 nm EB Lithography

Dielectric Sputter System

PLD

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Applied Materials (AMAT) Nanomanufacturing Laboratory

- AMAT is a leading semiconductor / photovoltaic equipment manufacturer
- Named Laboratory set up with state-of-the-art tools worth Rs. 41 crores
- Several joint research projects between AMAT & IITB
- 9 AMAT engineers/technicians stationed at IITB
- Donated equipment complements the CEN facilities

Gate Stack Centura

Etch Centura

Endura (PVD & PECVD)

INUP at IIT Bombay

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Punj ab University (4), Gurunanak University

Haryana College of Technology & management

CEERI Pilani(3), BITS Pilani, LMNIIT, Jaipur(2)

Nirma University of S&T, SVNIT,Surat, Gujarat University, Pandit Deendayal Petroleum University, Gandhinagar.(2) Visvakarma Govt Engg College

BARC(3),NCL Pune,CMET Pune
IISER Pune(2), University Pune,
VNIT Nagpur(2),SRKNEC Nagpur,
North Maharastra University
Larsen & Toubro,Piranhal Healthcare,Crompton Greaves

IISc Bangalore,
Applied Materials,
Tata BP Solar

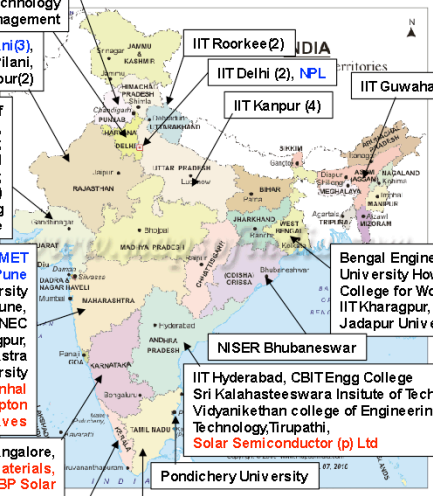
Amritha School of Engg., KUSAT

IIT Roorkee(2)

IIT Delhi (2), NPL

IIT Kanpur (4)

IIT Guwahati



Bengal Engineering and Science University Howrah(2), Vidyasagar College for Woman, IIT Kharagpur, University of Calcutta, Jadapur University

NISER Bhubaneswar

IIT Hyderabad, CBIT Engg College
Sri Kalahasteeswara Insitute of Technology, Sri Vidyanikethan college of Engineering and Technology,Tirupathi,
Solar Semiconductor (p) Ltd

Pondichery University

Anna University,Chennai(2),IIT Madras, KSR College Engg & Tech
VIT Vellore (2)

INUP user being trained by CEN staff

Total no. of users: 57
Academic: 45
R & D labs: 6
Industries: 6

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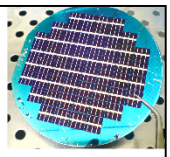
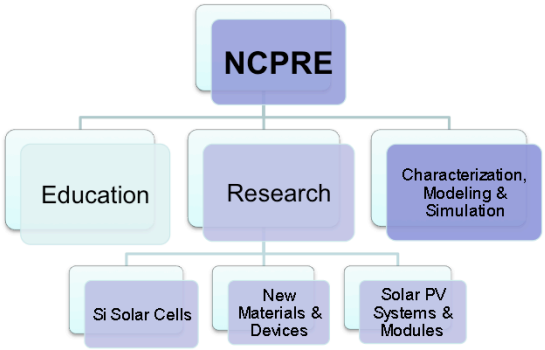
National Centre of Photovoltaic Research and Education





- 5 year funding of Rs. 47.5 crore from MNRE
- Part of Jawaharlal Nehru National Solar Mission (JNNSM) launched in January 2010: 20 GW from solar by 2022
- Strong Education + Research thrust
- Participation from several departments

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• W. Shockley, The path to the conception of the junction transistor, IEEE Transactions on Electron Devices, vol. 31, No. 11, 1986, pp. 1523

• I. Ross, The invention of the transistor, Proceedings of the IEEE, vol. 86, No. 1, 1998, pp. 7.

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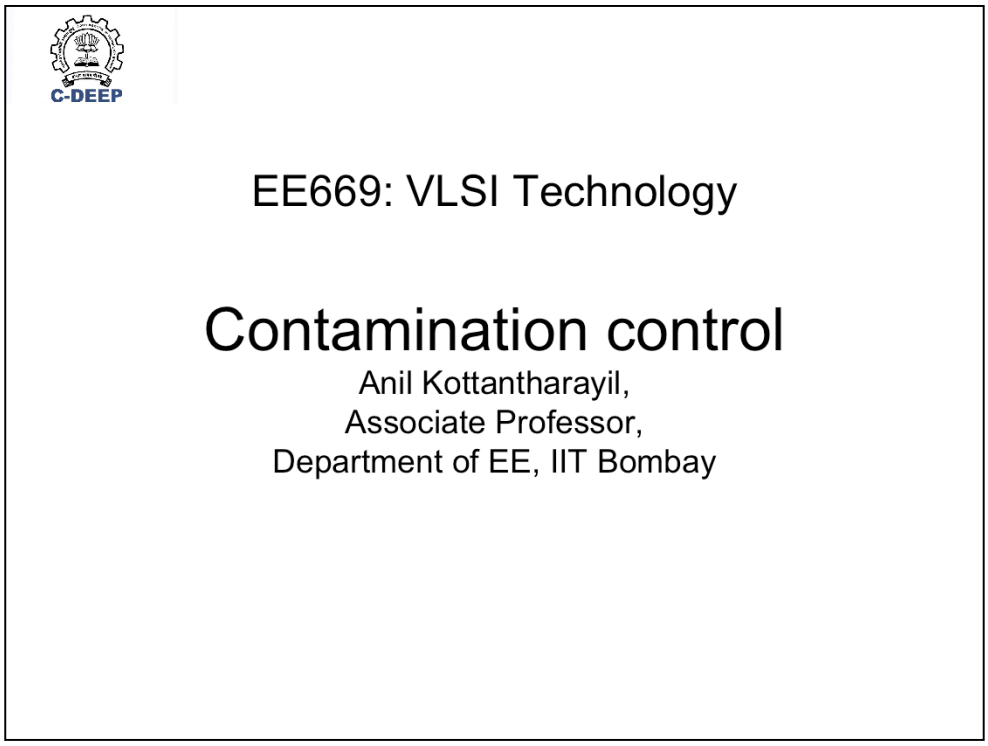
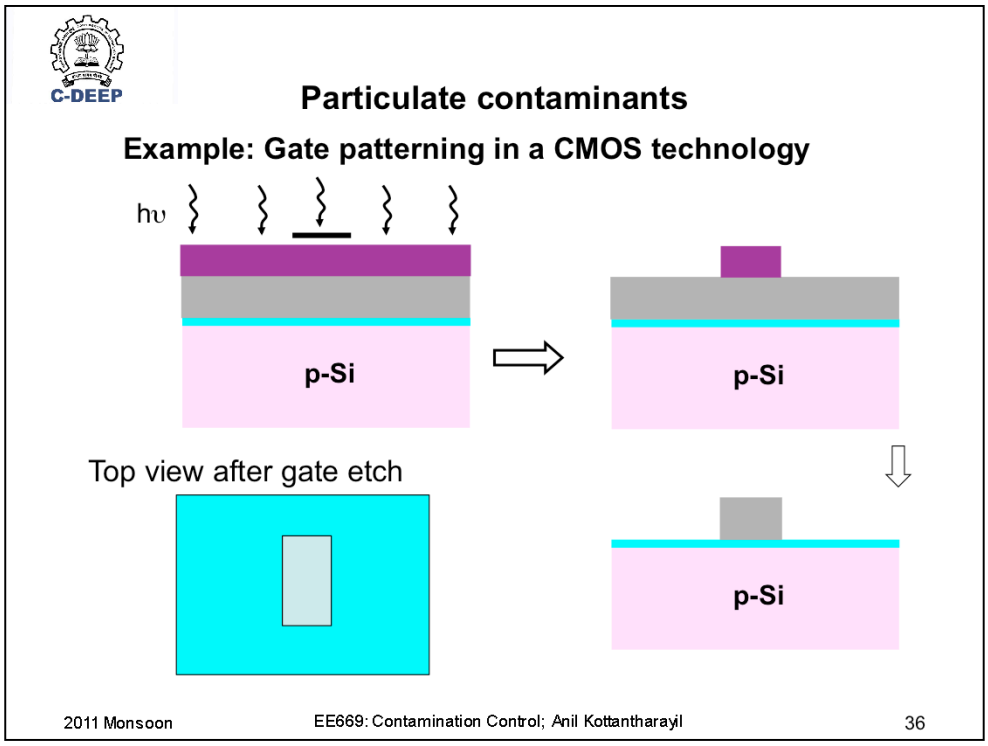


In the previous module where we had a peep at the history of the semiconductor engineering, we had seen an example of the transistor assembly line of late 1950's and early 1960's. However the yield, the devices or parts those functioned as per specification as a percentage of all the devices or parts made in the same processing lot, was quite low. Junctions made in those days had high leakage currents. Instability in device behavior had delayed the commercial exploitation of MOSFETs. The low yield, to a large extent could be attributed to contamination of the wafers during preparation, during processing and/or during packaging.

Contaminant can be defined as any material, the presence of which on the surface or in surface layers or in the bulk of the semiconductor that can result in a reduction in manufacturing yield. Contaminants can be particles from the environment that settle on the surface of the wafers during handling and processing or materials that can be incorporated in the device structures and the bulk of the semiconductor. We would review some of the implications of the presence of contaminants on VLSI technology.



We would deliberate the impact of particulate contamination on VLSI manufacturing using gate patterning process in CMOS technology.

The bottom left figure shows the top view of the wafer after etch of the poly Si and removal of the resist.

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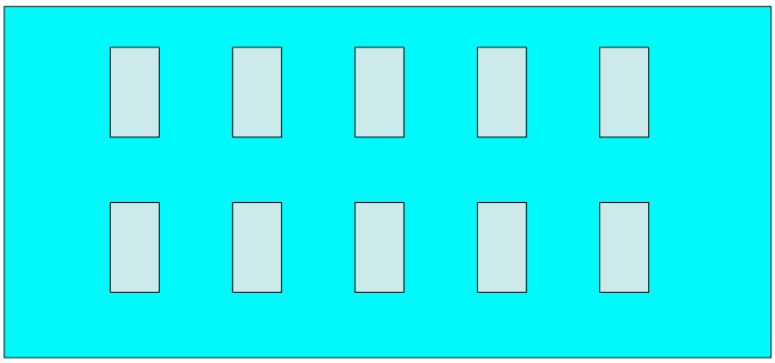
Particulate contaminants (2)



Several devices: Top view after gate etch.

This is what we want.

Let us say we want to make several such devices on the wafer. We would connect them together as per the circuit requirements to create an integrated circuit. This is how it should look after gate etch.

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Particulate contaminants (3)

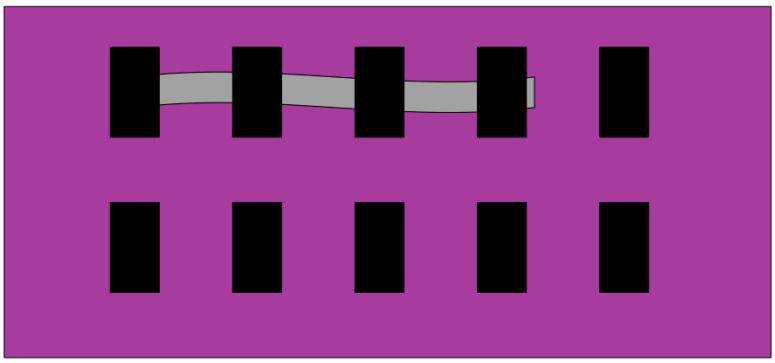

Photo resist with mask on top before exposure.

A particle, for example a piece of the hair of an engineer in the processing area falls on the wafer prior to the photo lithography process.

The first process is the photo exposure of the resist. Suppose a particle falls on the resist during the handling of the wafer. The particle, if opaque to the light used for exposure, would block the light from reaching the underlying resist.

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Particulate contaminants (4)

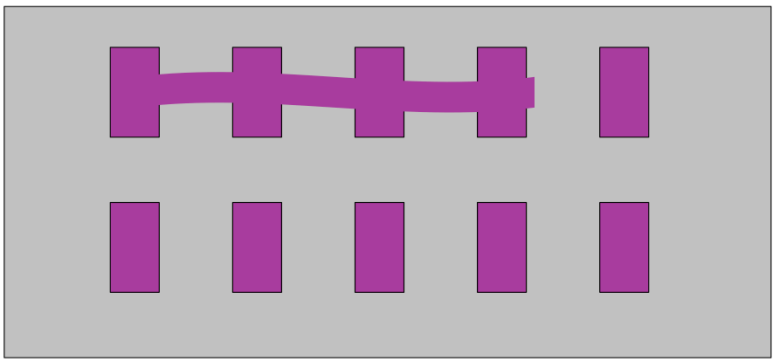

Photo resist after exposure and development.

As a result, after development, the resist would look like this.

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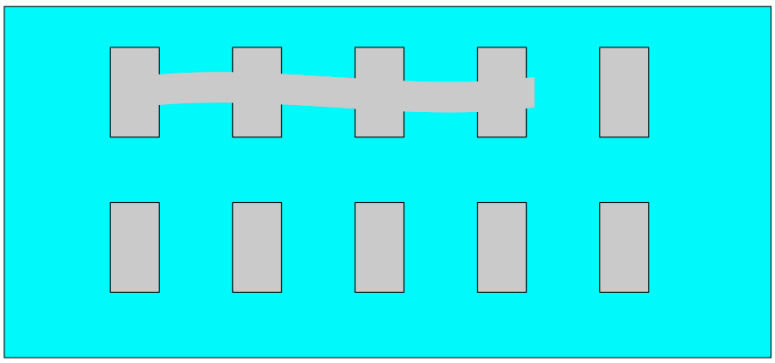
Particulate contaminants (5)



Poly Si gates after etch of poly Si and removal of the resist.

The contaminant particle has caused a short between several gates and if the circuit design does not require this, we would have an integrated circuit that would not work. This can happen in any lithography process. Particulate contamination can also be fatal for the IC if it happens during gate oxidation, thin film deposition etc.

The IC is likely to work satisfactorily if the size of the particle is smaller than the minimum feature sizes in the IC. More over there may be some parts of the circuit where the features are larger than the smallest, or which contain non critical sections of the circuit etc. These considerations imply that the yield of ICs can be improved by reducing the particle count in the environment in which the ICs are manufactured.

With ever decreasing feature sizes in ICs, particle contamination control is very important in semiconductor manufacturing to obtain high yield. Lithography places the highest demands on the particle control, mainly dictated by the fact that feature sizes are decided by lithography processes. A typical state of the art chip fabrication process may involve 30+ lithographic processes.

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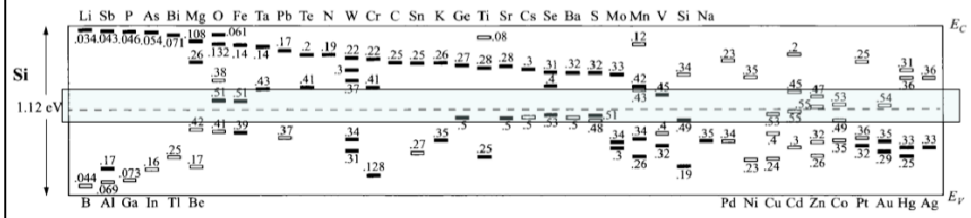
Metallic Impurities (1)



S. M. Sze, Physics of Semiconductor Devices

These are efficient generation – recombination centers

$$\tau = \frac{1}{\sigma v_{th} N_t}$$

- Cause high reverse bias leakage in diodes
- Reduction of bulk lifetime - carrier collection in solar cells would be reduced – reduced power conversion efficiency

The figure shows the simplified band structure of Si and various energy levels in the forbidden gap introduced by impurities in Si. You may learn more about the physics of this in the device courses. You may note the energy levels introduced by the commonly used dopants for controlling conductivity. The defect levels at the middle of the bandgap are very efficient in generation and recombination processes.

It suffice to know that the carrier life time, the average time that a carrier is “alive” in the semiconductor, in the case of Si depends inversely on the density of traps, N_t. Let us say we have Au in Si. N_t ~ concentration of Au.

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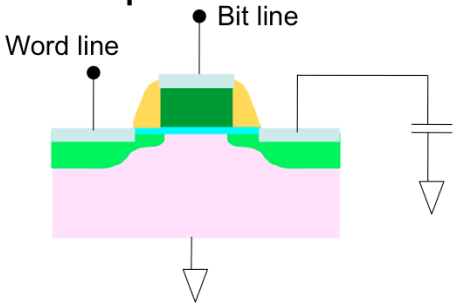
Metallic Impurities – life time killers (2)

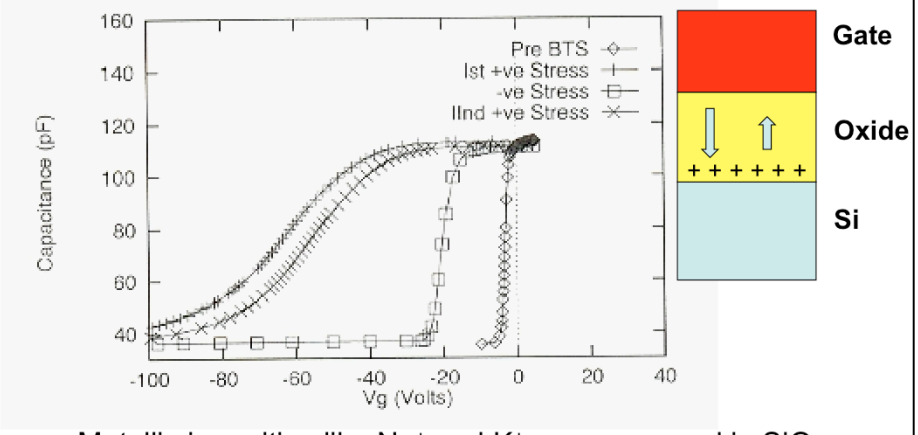


Impurities can cause high reverse bias leakage in diodes

$$J = \frac{qn_i W}{2\tau} = \frac{1}{2} qn_i W \sigma v_{th} N_t$$

- When the capacitor is charged to ~ V_{DD}, and holding logic 1, the source to substrate junction is reverse biased.
- Leakage determines how often the DRAM cell has to be refreshed.

Metallic Impurities – ionic mobile charge (3)



• Metallic impurities like Na^+ and K^+ moves around in SiO_2 under electrical field causing instability in characteristics.

K. G. Anil, M. Tech thesis, IIT Bombay

MOS structure is the heart of the MOSFET and it consist of a metal gate, insulator (Silicon dioxide) and Silicon. The field effect transistor is highly sensitive to any charges near the surface. Mobile ions in the dielectric can move around in the semiconductor. This would cause a shift in the capacitance – voltage characteristics of the MOS capacitor (shown) and a corresponding shift in the threshold voltage of the MOSFET.

$\Delta Vt = -Q_M/C_{OX}$

Where Q_M is the mobile charge density in Coulomb per cm^2 and C_{OX} is the oxide capacitance per cm^2.

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Tackling contamination

Three strategies:

• Specially designed low particle count clean rooms for manufacturing and R & D. Particle control during processing.

• Strict delineation of processes as clean and contaminating and intermediate process steps to avoid contamination. **Wafer cleaning procedures** between such steps to remove contaminants.

• Impurity gettering to handle contaminants, especially metals, incorporated in the wafer during processing.