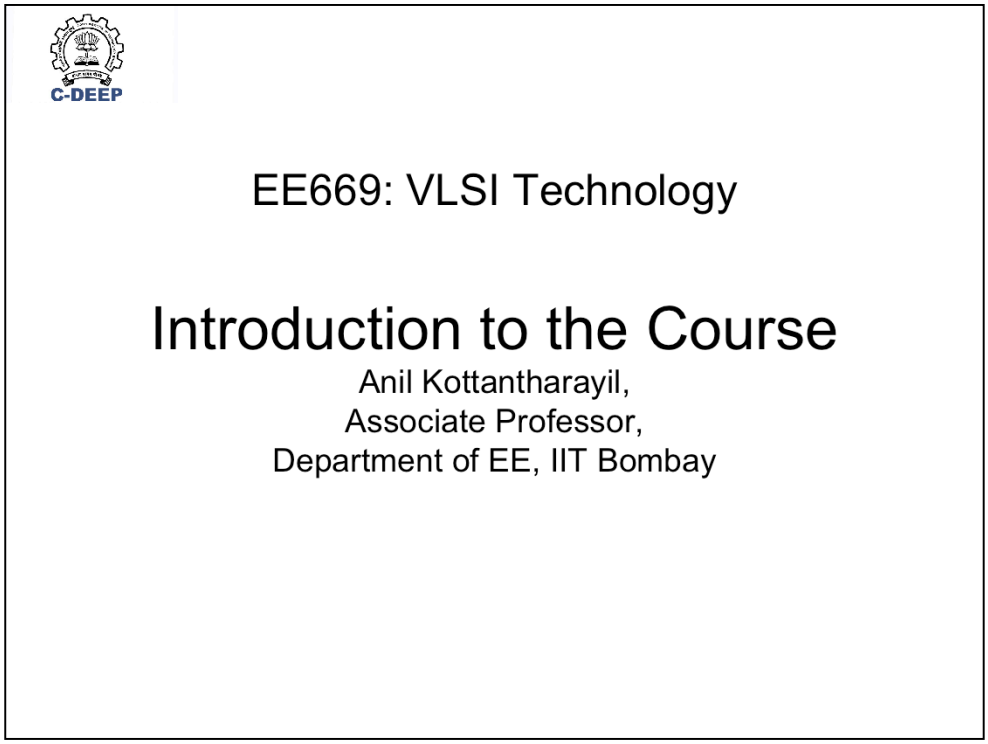


Introduction to the course. In this lecture I would try to set the course in perspective. Before we embark on learning something, it is good to ponder why it would be interesting, besides the fact that it can fetch useful course credits.

What do you understand by VLSI? In retrospect, integrated circuits having 10s of devices were called small scale integrated circuits (SSI), a few hundreds were called medium scale few thousands large scale. The game stopped with VLSI as people lost the count (not really). What does the word VLSI bring to your mind? Discussion to follow.

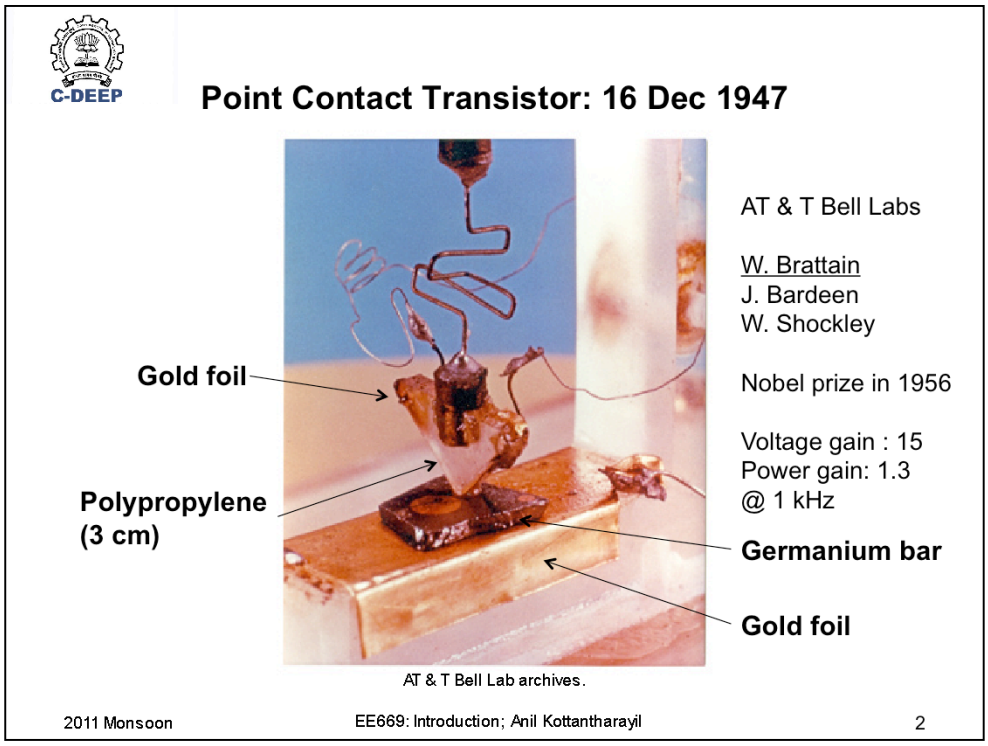
What do you understand by technology? Discussion to follow. Technology is the application of scientific knowledge for practical purposes. For example, why you may not call VLSI circuit design as VLSI technology? This is by convention in the semiconductor business research and business community. The convention is to treat fabrication technology as the “technology”.

In this course we would discuss and try to learn how Silicon Integrated Circuits are fabricated. Integrated circuits are fabricated by a sequence of fabrication steps called unit processes. A unit process would add to or subtract from a substrate. Examples of unit processes can be cleaning of a wafer, deposition of a thin film of a material and so on. The unit processes are not uniquely applied to VLSI fabrication only. I can combine several of these unit processes to make solar cells. I can do same for making MEMS devices. So the unit processes can be thought of as pieces in a jigsaw puzzles. The outcome would depend on how you sequence the unit processes.

In a toy jigsaw puzzle, the jigsaw pieces have well defined edges. However in our jigsaw puzzle of making semiconductor devices and circuits, the pieces are going to influence each other. These interactions can profoundly change the existing structures or features on the already build part of the circuit. So integration of unit processes should be done with good care and you need a good understanding of the unit processes, their interactions and potential impact on the eventual circuit made. So in this course we would analyze some of the integration schemes used in the industry and try to gain some insight into the art called process and device integration.

That is the satellite view of the course, of course the satellite we use a metaphor was made before the advent of the VLSI era.

In this lecture we would go back into history and see how the first transistor was made. That would allow us to appreciate the growth in aspirations, ambitions and complexity associated with present day VLSI technology.



The very first idea for a transistor was proposed by Julius Edgar Lilienfeld in a Canadian Patent titled "Electric current control mechanism". CA 272437 (A) – 1925. Lilienfeld filed several patents on transistors in the 1920s. However it took several years before transistors could be constructed and demonstrated. In early 1940s a research team was setup in AT & T Bell labs with the objective to make an electronic switch that would replace mechanical relays in telephone exchanges. The leader of the team, William Shockley wanted to make a device in which the the conductivity of a semiconductor surface can be controlled by an electric field. The team came up with the transistor shown. Interestingly this device does not work on the concept of field effect the team set out to make. But it worked.

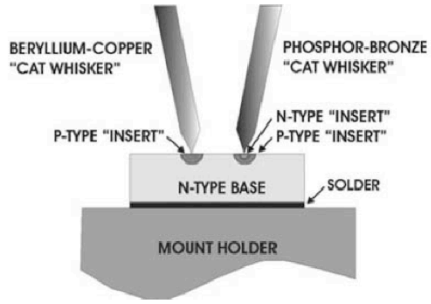
How was the device constructed? The fabrication procedure was the idea of Walter Brattain. The triangle shaped piece is made of polypropylene and a gold foil is pasted to the wedge of the plastic piece. The gold foil is contacted at the two upper ends. The gold foil is slit at the tip of the triangle using a sharp razor. The whole assembly is then pressed against the surface of a high resistivity n-type Ge bar using a spring. The Germanium in turn is glued to a gold foil using some conducting paste. The two gold contacts at the top are the emitter and collector contacts of the transistor and the Germanium bar is the base of the transistor.

You may recognize the symbol of the bipolar junction transistor in this construction. However this is not a bipolar junction transistor. The gold makes Schottky contacts to Germanium.

The device structure was derived from suggestions by John Bardeen and Robert Gibney. Shockley did not have any significant contribution to this invention. However he tried to develop a theory of the device, could not really do it. Instead he proposed the bipolar junction transistor and developed the theory of BJT. BJT was constructed in subsequent years.

C-DEEP

Type A Point Contact Transistor: 1948



W. G. Pfann's improved point contact transistor, AT & T Bell Labs, 1948.

Bo Jolek, History of semiconductor engineering, Springer, 2007.

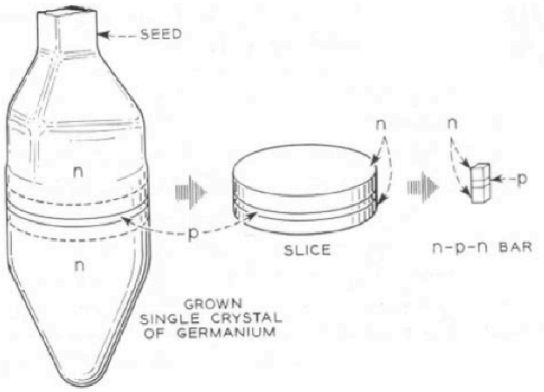
As you can appreciate, the fabrication method used for the first point contact transistor is difficult to put into large scale manufacturing. The main problem is how to control the size of the slit which decides the gain of the transistor. However the fabrication is very simple. No two transistors behaved the same way.

An improved method using cat whiskers of Beryllium-Copper and Phosphor-Bronze was developed by W. G. Pfann of Bell labs. The packaged device can be seen on the right.

The contacts are pressed by the spring action of the whiskers. An electrical stress is applied at the terminals which resulted in converting the contacted Germanium regions into p-type, by the diffusion of Cu during the electrical stress. The right hand contact would also have have phosphorous diffusing into the Ge. The device is then a PNPN thyristor. The spacing between the two contacts are "controlled" to some extent by a spacer between the two spring assemblies.

C-DEEP

Grown bipolar junction transistors



Grown junction Bipolar Junction Transistors made by Morgan Sparks at AT & T Bell labs in 1950.

Bo Jolek, History of semiconductor engineering, Springer, 2007.

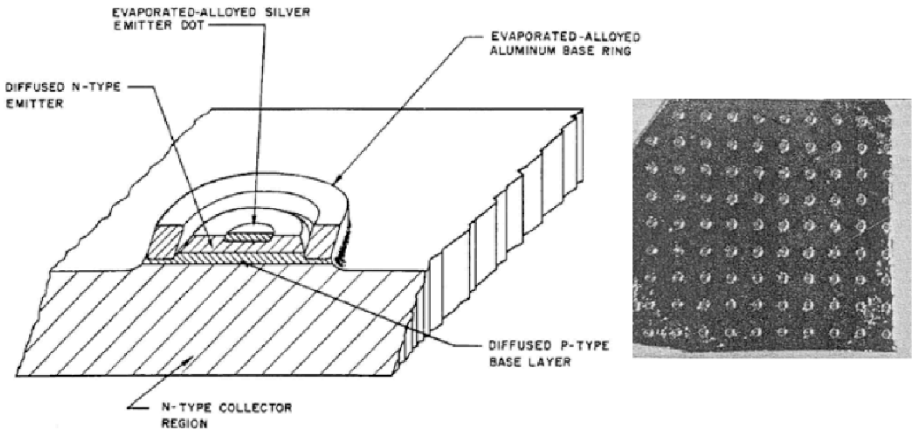
One of the first BJT to be fabricated was the grown junction transistor. This was made by Morgan Sparks at Bell Labs.

Here we start to see some of the unit processes still being used in Silicon technology. You may note that the point contact transistor fabrication did not involve any thermal processes. Of course the crystals were grown using thermal processes.

The material used here is Germanium. A Germanium seed is inserted into molten Germanium doped n-type. The seed crystal is pulled so that crystalline Germanium grows as shown. At certain stage p-type dopants are added to the melt. Subsequently a higher concentration of n-type dopants are added to the melt. This would result in the Germanium ingot shown. The transistors are sliced into individual pieces as shown. The thickness of the base was in the range of 100 to 25 um. The transistor worked upto 20 kHz.

C-DEEP

Mesa junction transistors



Lew Miller, Western Electric in 1958.

Bo Jolek, History of semiconductor engineering, Springer, 2007.

An N-type Silicon was the starting material. Gallium Trioxide (Ga_2O_3) source was used for p-type doping of the wafer. Subsequently n-type diffusion from Phosphorous pentoxide (P_2O_5) was carried out through a metal hard mask. Mesas were etched by wet etch processes to expose the base layer for contacting. Al evaporated through a hard mask was used for contacting the base. Silver was used to contact the emitter. The device was then mounted on a Gold platted package mount and Gold wires were bonded to the emitter and base.

As you can see on the right hand side, large number of devices can be made on semiconductor wafers simultaneously. This process allowed the production of mass manufacturing of transistors.

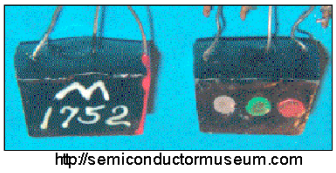
C-DEEP

Applications of Transistors

- Several that you already know
- And some that you probably did not know

including

"In the early fifties it was quite fashionable for ladies in the Murray Hill neighborhood to use transistors as colorful jewelry." Bo Jolek, History of semiconductor engineering, Springer, 2007.



http://semiconductormuseum.com

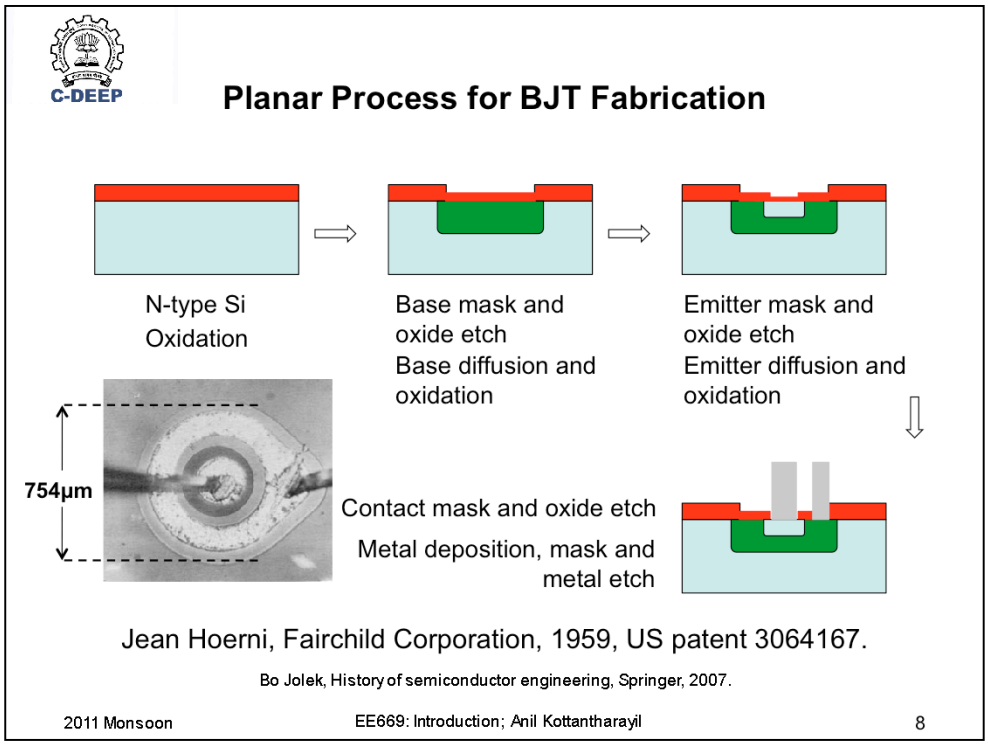
What are applications of transistors?

Some of the early transistors were colorfully packaged.

The packaged transistor shown is M1752 from Bel labs.

Early Stage Transistors: features

- Simple fabrication process by today's standard
  - you could make the point contact transistor of Brattain at home with not so sophisticated tools in about an hour with a rather short bill of materials
- No two transistors worked the same way, if at all they worked – low yield
  - The cut in the gold foil or spacing between whiskers are difficult to control – point contact transistors
  - Exposed semiconductor surfaces resulted in uncontrolled characteristics
  - Processing not done in clean rooms – large defect density
- Pricy: In 1958, Fairchild sold 100 transistors to IBM for $ 150 a piece (inflation adjusted 2011 equivalent ~ $ 1050 per piece!)



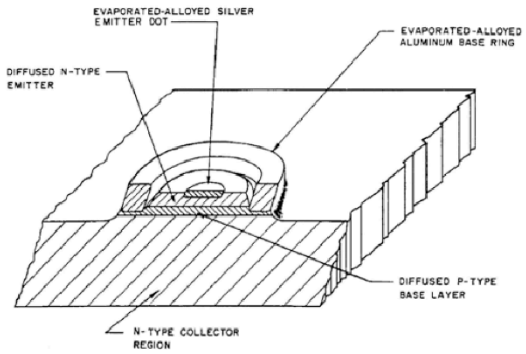
An invention that changed the scene was the planar process for BJT fabrication. Jean Hoerni of the Fairchild Corporation is credited with this invention. This is an important precursor of the integrated circuit technology.

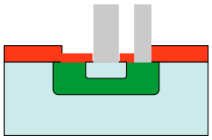
The process is well described by the animated schematics. An important feature here is the use of SiO2 as a mask against diffusion an important breakthrough in semiconductor technology. However this is not attributed to Hoerni. Another factor is the fact that semiconductor surfaces are not exposed post fabrication. The surface of any material is sensitive to the ambient as it can go through chemical changes, undesired materials can be deposited, etc. The previous versions of transistors always had semiconductor surfaces exposed to the surrounding. For example, the mesa transistor base to collector junction is exposed. The junction is reverse biased in active mode and should sustain large reverse bias.

Planar processing has a highly desirable feature in the the surface is mostly on one plane. You would learn that this is a very important aspect which enables high resolution lithography.

C-DEEP

Planar Process: the key difference from previous processes





- Semiconductor surface is not directly exposed to ambient in a device obtained using the planar process – lower leakage, higher breakdown voltage and better stability
- Large scale manufacturing of bipolar junction transistors with high yield possible using the planar process
- Precursor to integrated circuits

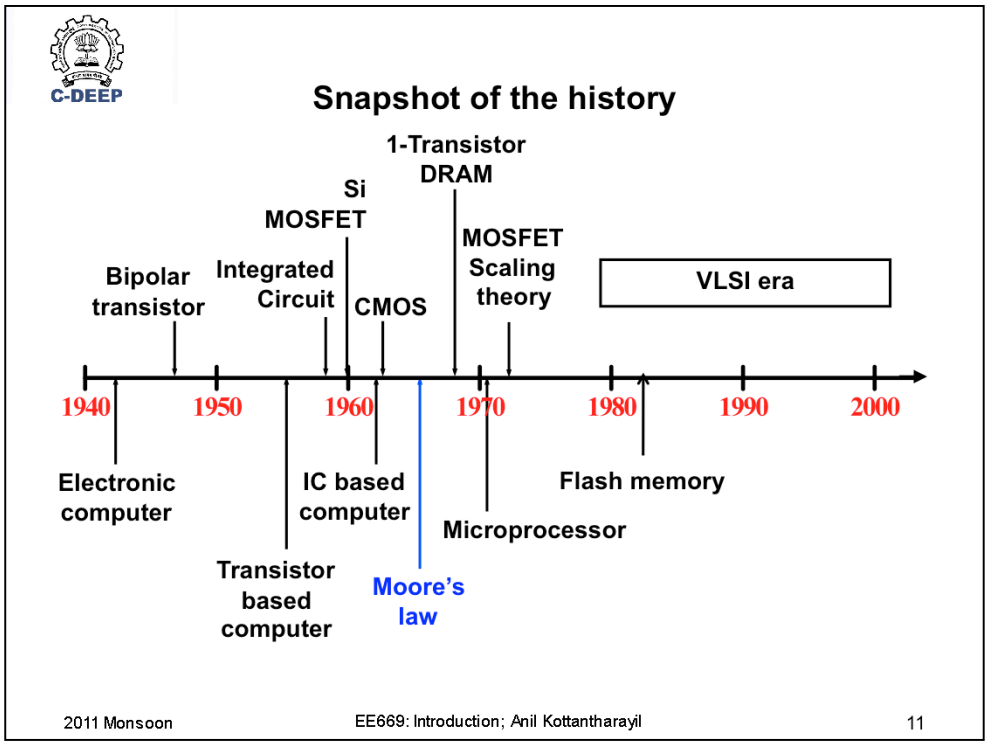
C-DEEP

Transistor assembly line of late 1950's

Bo Jolek, History of semiconductor engineering, Springer, 2007.

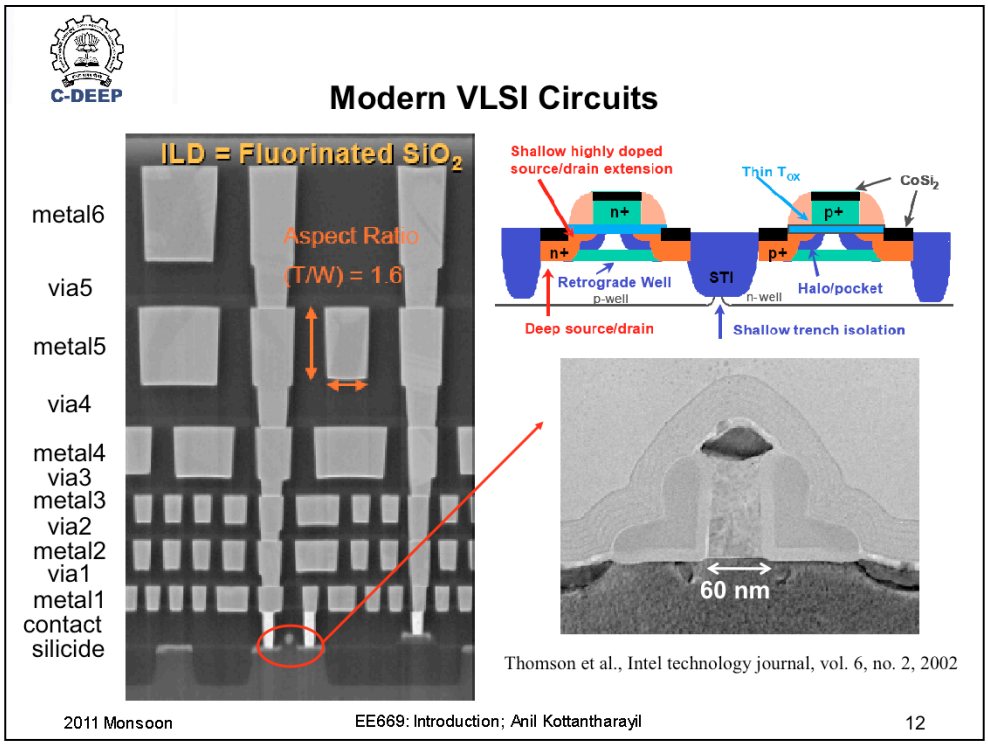
The figure shows a transistor assembly line of the 1950's. Note that the transistors were assembled by hand and not in restricted and controlled environments. VLSI circuits are fabricated in highly automated ultra clean manufacturing lines.

The history of semiconductor engineering is very exciting. We have looked at only a few of the examples of early devices. If you are interested to probe further I can recommend the book by Bo Jolek. The book looks at the history from a US angle and has given interesting insights into the beginning and progress of the field. How inventions were made, entrepreneurs struggled, and discusses very colorful personalities who were more colorful than the transistors we had seen. The books skips most of the activities in Europe and Japan that have also contributed significantly to the progress in the field. However it is a compelling book.

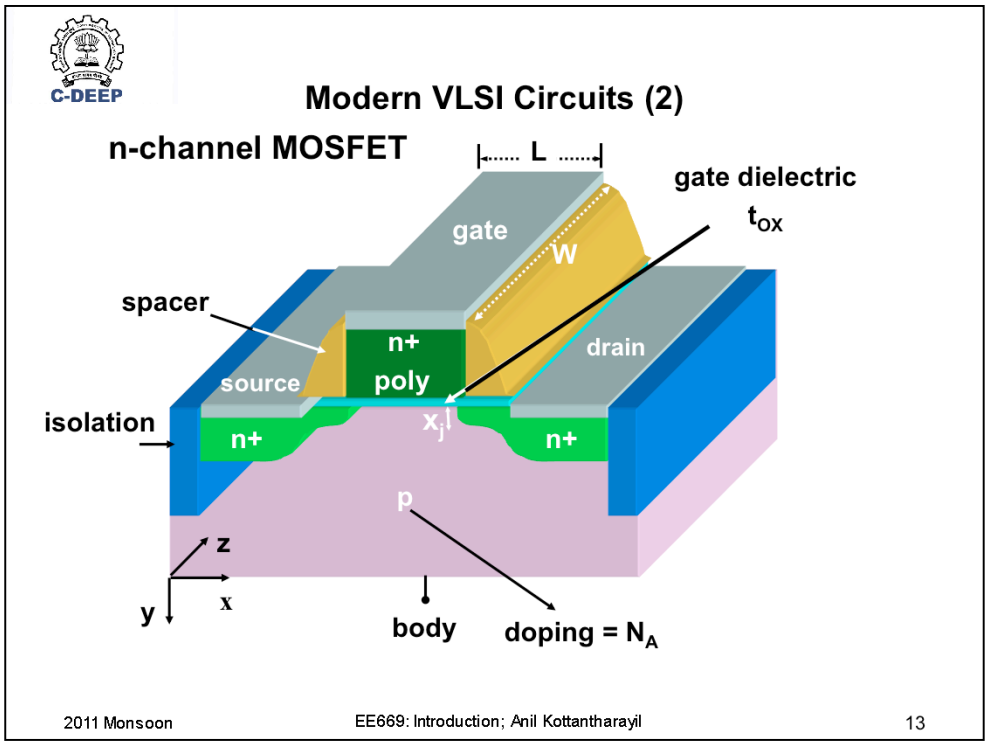


1. First vacuum tube: 1904, John Fleming, UK.
2. Proposal of field effect transistor, no proof of realisation: 1925, Lilienfeld, USA
3. First electronic computer ABC: 1942, J. V. Atanasoff and C. Berry, Iowa State University, USA
4. ENIAC: J. P. Eckert and W. Mauchley, University of Pennsylvania, USA
5. Bipolar transistor: 1947, Shockley, Bardeen and Brattain, AT&T Bell Labs, USA
6. First transistor based computer: 1956, Bell labs, USA
7. Integrated circuit: 1958, R. Noyce of the Fairchild corporation, Monolithic IC. Jack Kilby of Texas Instruments, hybrid integrated circuit.
8. Silicon MOSFET: 1960, Kahng and Atalla, Bell Labs.
9. First computer with IC: 1962, Digital Equipment Corporation
10. CMOS: 1963, Wanlass and Sah, Fairchild, USA.
11. Moore's Law: 1965
12. One transistor DRAM cell: 1968, Dennard, IBM, USA
13. Microprocessor: 1971, Intel corporation, USA
14. MOSFET scaling theory: 1973, Dennard, IBM, USA

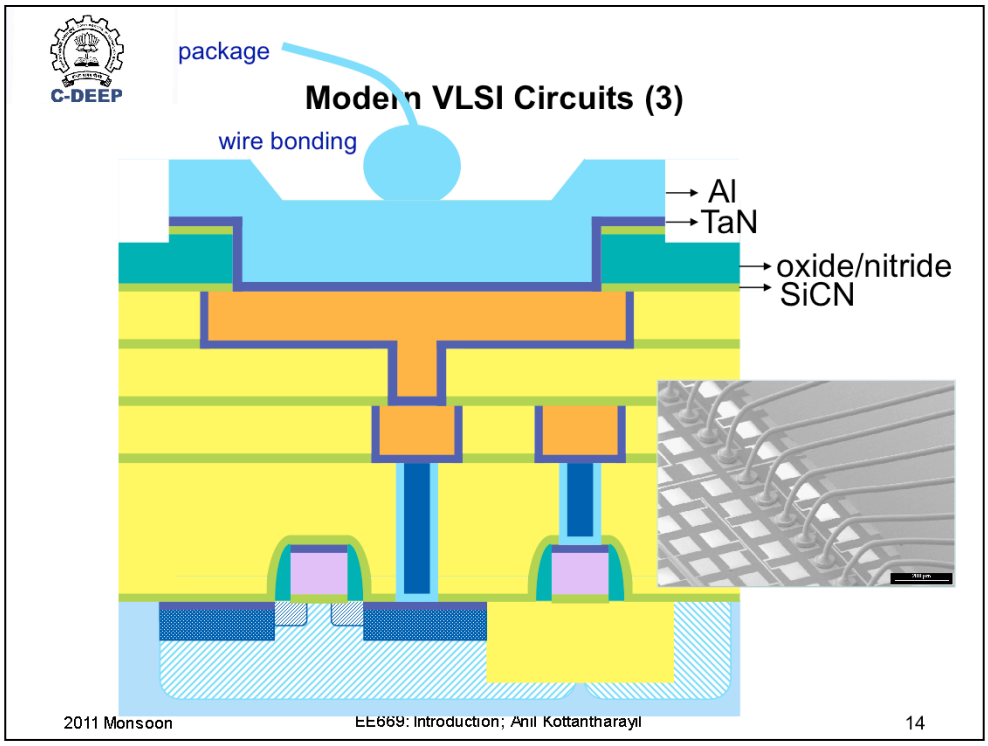
This slide essentially captures some of the key inventions that we discussed and those followed. The time from Dennard's scaling theory in 1973 to 2007 was called the happy scaling era of VLSI by some of the experts as there were no radical and noteworthy concepts that influenced the scaling. However since 2007 the industry has seen the introduction of non SiO2 gate dielectric and non planar device architectures.



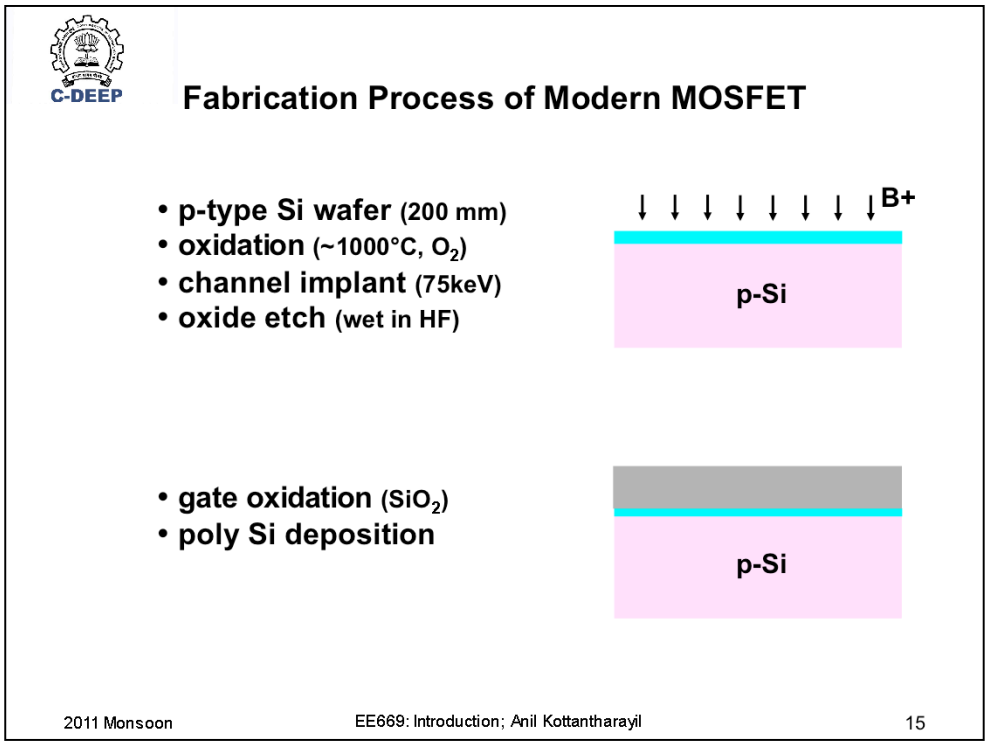
This slide shows how a real modern VLSI circuit looks. The left side figure shows the cross section secondary electron micrograph (SEM) of a VLSI chip. You can see the top of VLSI chips on the wafer that is being passed around. The transistor is the tiny bit low down highlighted by the red oval. The light gray blocks are the interconnects for wiring together devices to make circuits. The darkest shade in the figure is the isolation between the devices and between the devices and the interconnects. This is typically some form of Silicon oxide. The processing is planar, in that each step is done on a fairly planar surface (remember Hoerni's transistor). The cross section SEM of the transistor is shown on the right bottom of the slide. The gate length is about 60nm (prototypes in year 2002). Compare this to the first transistor, the dimensions were in the range of 3 cm, a 50000X reduction in size in 55 years.



A closer 3D schematic of the n-channel MOSFET in modern VLSI circuits is shown on this slide.



A chip of course has to be connected to the external world and connections are bonded to the chip.

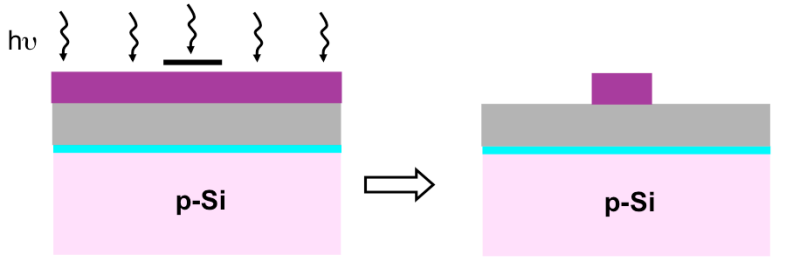


Now we would look at the process flow for fabrication of a MOSFET in a typical VLSI process. We would not discuss the full fabrication of a VLSI circuit. That is a topic we would discuss later in this course. This is just to give an idea and also you may find it useful to compare the fabrication process used for early transistors.

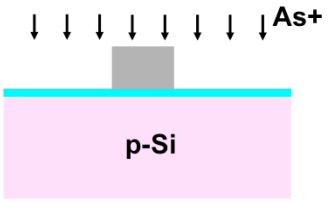
C-DEEP

Fabrication Process of Modern MOSFET (2)

- gate optical lithography



- gate etch (anisotropic)
- resist removal
- S/D implant 1 (extensions)

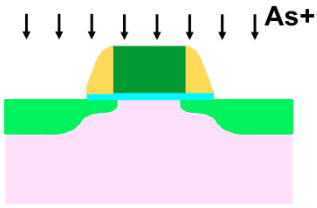


C-DEEP

Fabrication Process of Modern MOSFET (3)

- spacer, Si_3N_4 (anisotropic etch)

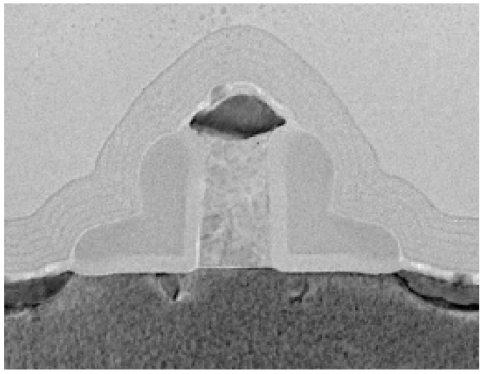
- S/D implant 2



- Ti/Co/Ni silicide

C-DEEP

Fabrication Process of Modern MOSFET (4)



C-DEEP

Reference books

- Bo Jolek, History of semiconductor engineering, Springer, 2007.
- J. D. Plummer, M. D. Deal, P. B. Griffin, Silicon VLSI Technology, Pearson Education, 2001
- S. K. Ghandhi, VLSI Fabrication Principles, Wiley Interscience, 1983
- S. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2001