Mixed-Signal VLSI Design
Course Code: EE719
Department: Electrical Engineering
Lecture 11: February 04, 2020

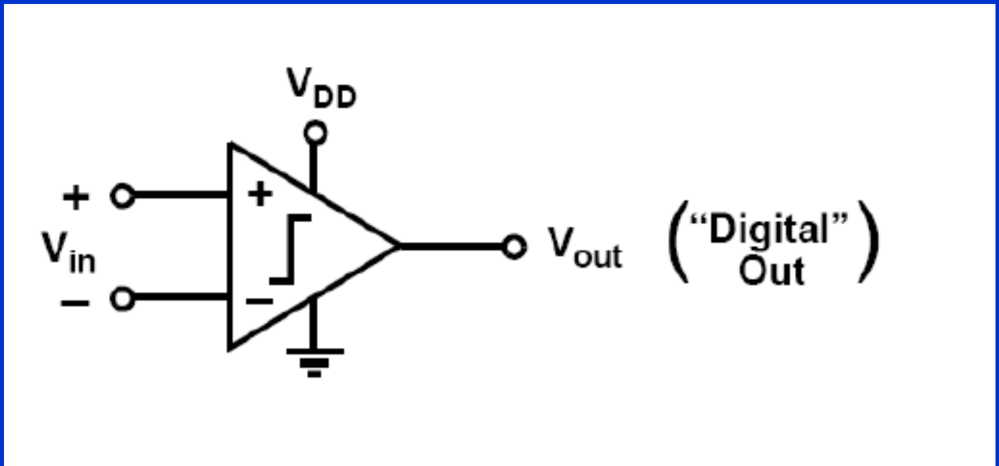
Instructor Name: M. Shojaei Baghini
E-Mail ID: mshojaei@ee.iitb.ac.in

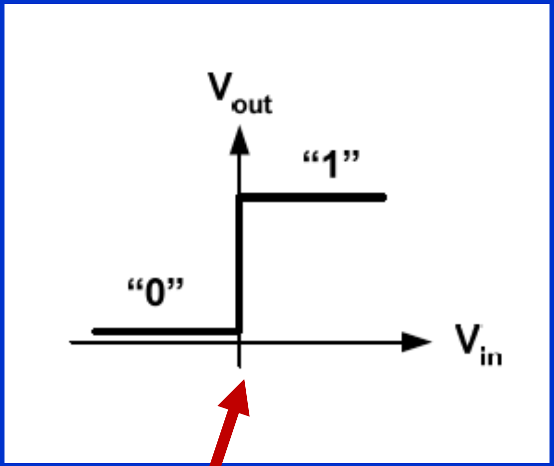
Module 11
Introduction to the Comparators

References

- Prof. Boris Murmann's slides from "VLSI Data Conversion Circuits", Stanford University, 2013.
- Section "Latched Comparators" onwards from chapter "Comparators", Analog Integrated Circuit Design by T. C. Carusone, D. A. Johns and K. Martin, J. Wiley & Sons, 2012.
- "Clocked Comparator" from chapter "Submicron CMOS Circuit Design", CMOS Mixed-signal Circuit Design by R. Jacob Baker, Wiley India, IEEE press, reprint 2009.
- "Comparator" from chapter "Nonlinear Analog Circuits", CMOS Circuit Design, Layout and Simulation by R. Jacob Baker, Wiley India, IEEE press, 2008.
- "The StrongArm Latch", B. Razavi, IEEE Solid-State Circuits Magazine, Spring 2015.

Ideal Voltage Comparator





Infinite gain!

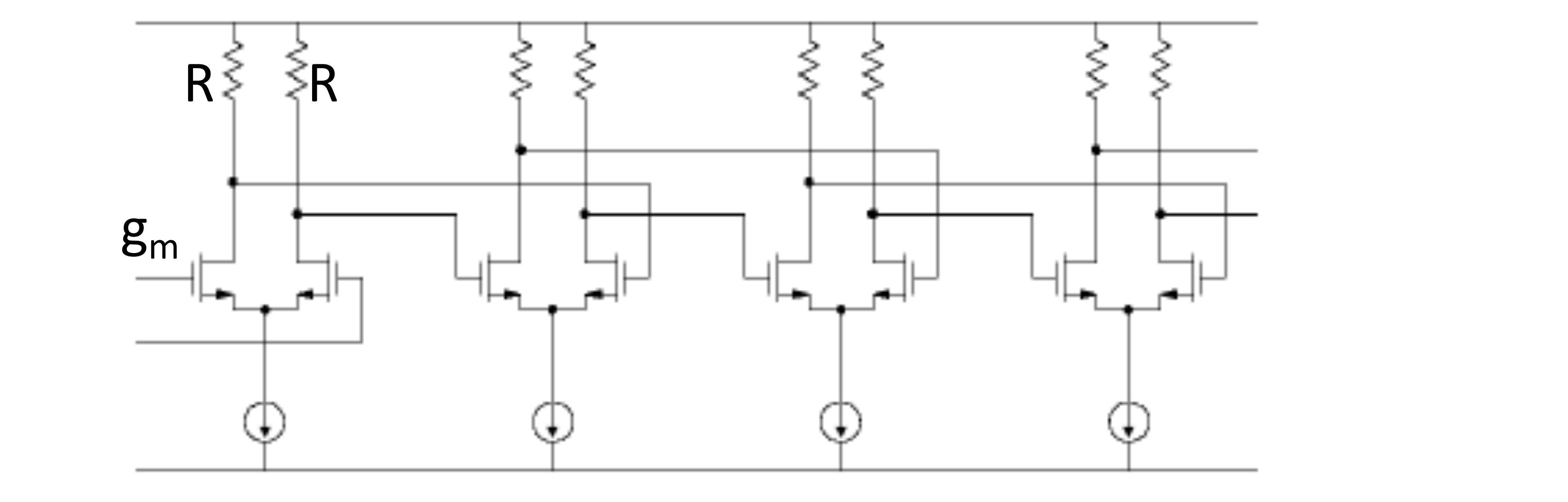
- High gain but not necessarily linear amplification
- Amplification can happen in discrete time.
- Clocked versus un-clocked comparator

Realization of High Gain Operation

- Common Technique for Amplifiers: Cascade of Stages

- Amplification can happen in the form of a regenerative process due to positive feedback

Cascade of Gain Stages



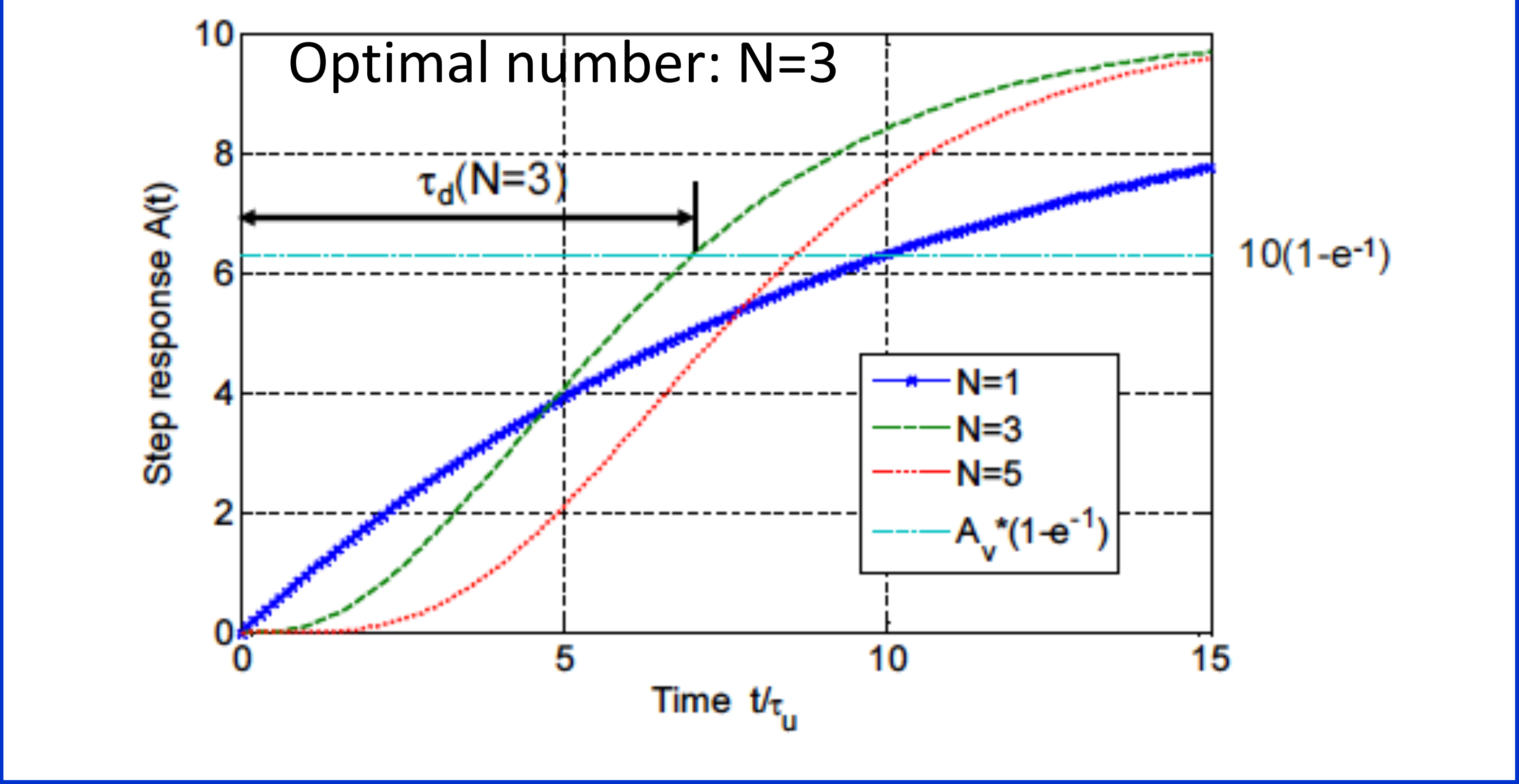
N: Optimal number of stages

$A_{v0} = -g_m \times R$, $A_v = (A_{v0})^N$, $BW_0 = \frac{1}{RC} = \frac{1}{\tau} = \frac{1}{A_{v0}\tau_u}$ where $\tau_u = \frac{C}{g_m}$

and C is the equivalent C observed at the output of each stage.

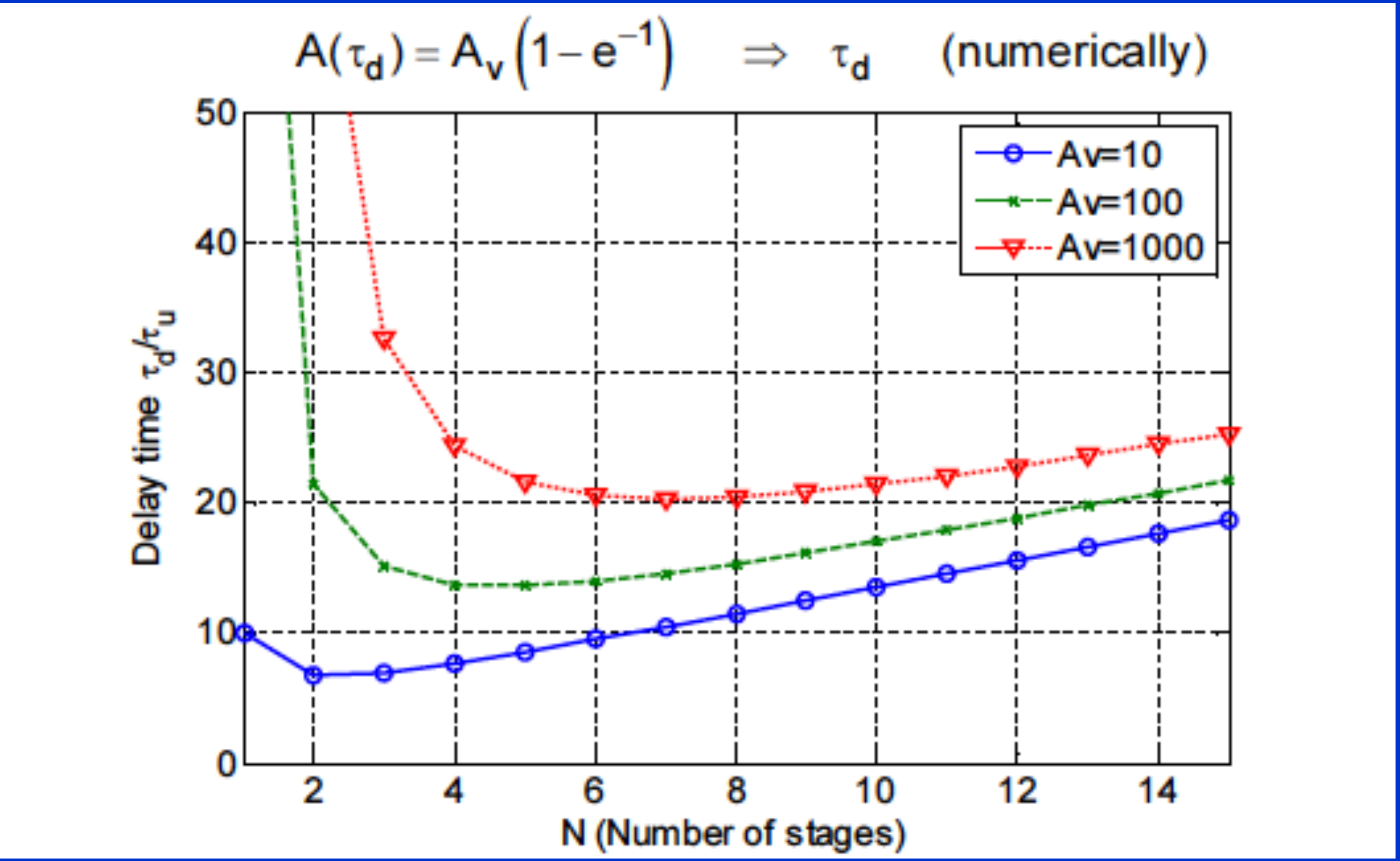
$$V_{out}(s) = V_{in}(s)A_v(s) = \frac{\Delta V_{in0}}{s} \times \frac{A_v}{\left(1+A_v^{\left(\frac{1}{N}\right)}\tau_u s\right)^N}$$

Step Response of the Multi-stage Amplifier with A_v=10



B. Murmann's course, Stanford univ., 2013

How does minimum delay change with increasing A_v?



B. Murmann's course, Stanford Univ., 2013

Analytical Derivation of the Optimum N

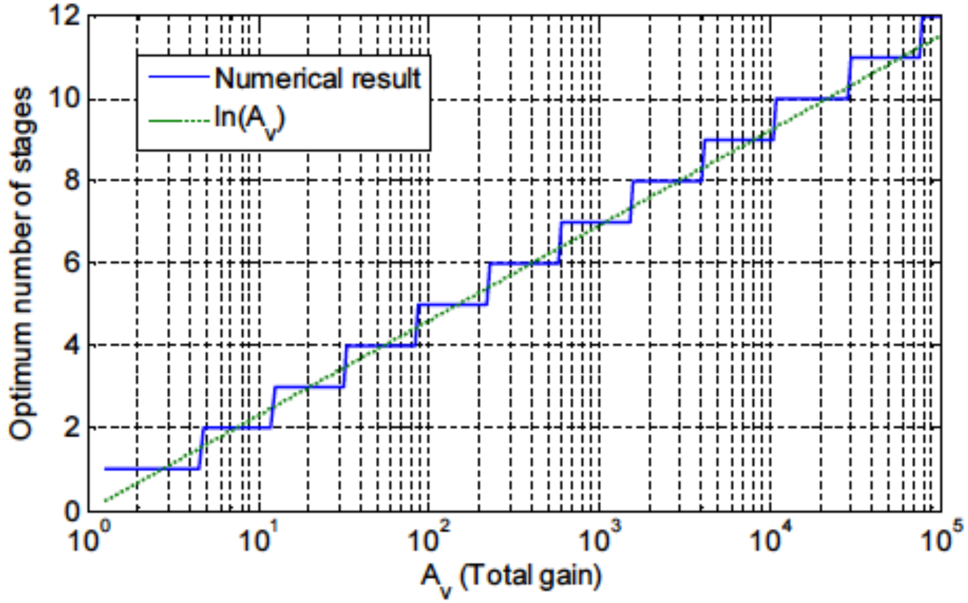
$A_v = (A_{v0})^N$, $t_d \approx N \times \tau_u \times A_{v0} = N \times \tau_u \times A_v^{1/N}$

$dt_d/dN = 0 \Rightarrow A_v^{1/N} - \frac{1}{N^2}(ln(A_v))N\, A_v^{1/N} = 0 \Rightarrow$

$N_{opt} \approx ln(A_v)$, $A_{v0} = e$, $t_{d,min} \approx ln(A_v) \times \tau_u \times e$

$e \approx 2.7$

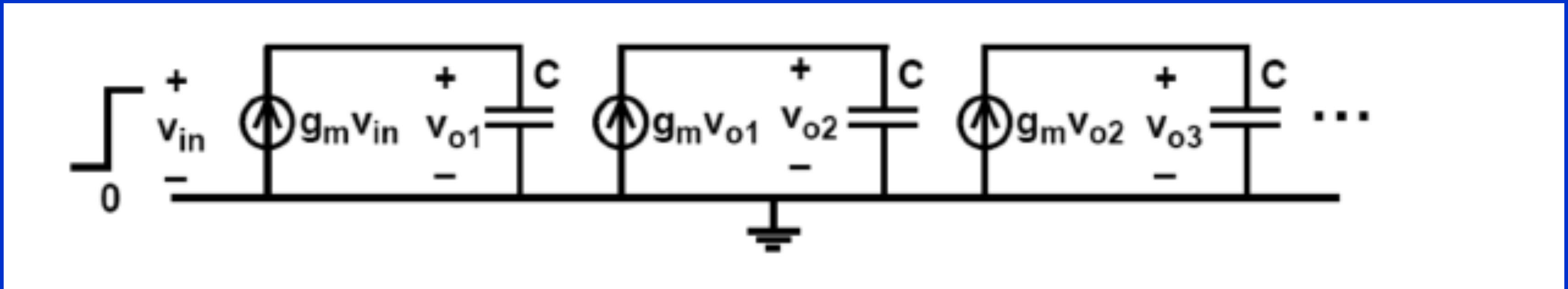
Similar to logic effort-based buffer design!



$N_{opt} \cong ln(A_v)$

Improving the Performance of Each Stage

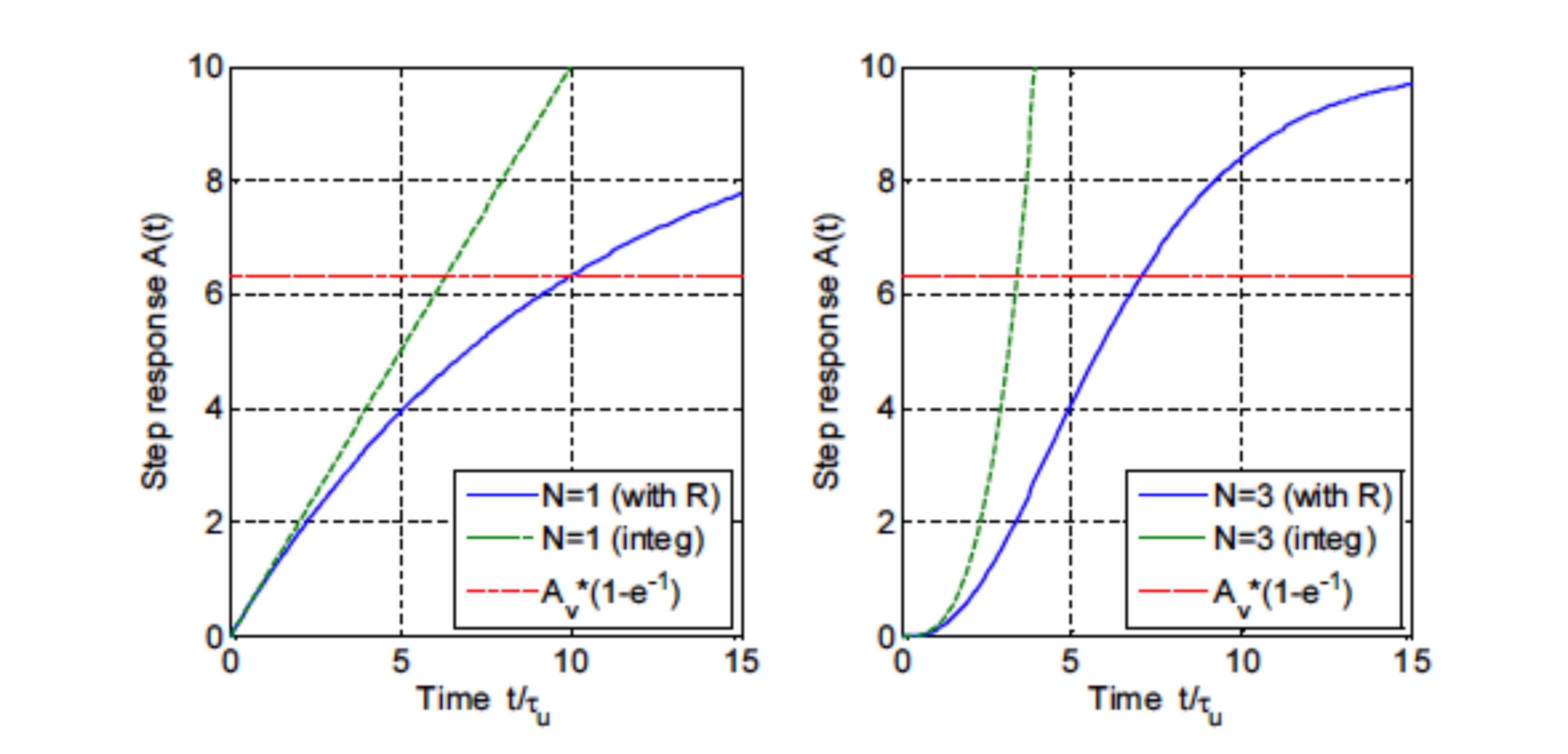
Removing resistors helps to feed the entire current to the capacitors (i.e. only capacitive load as opposed to RC load).



B. Murmann's course, Stanford Univ., 2013

Performance Improvement using Integrator

There is no limit for the final output but practically supply voltages will limit it.



B. Murmann's course, Stanford Univ., 2013

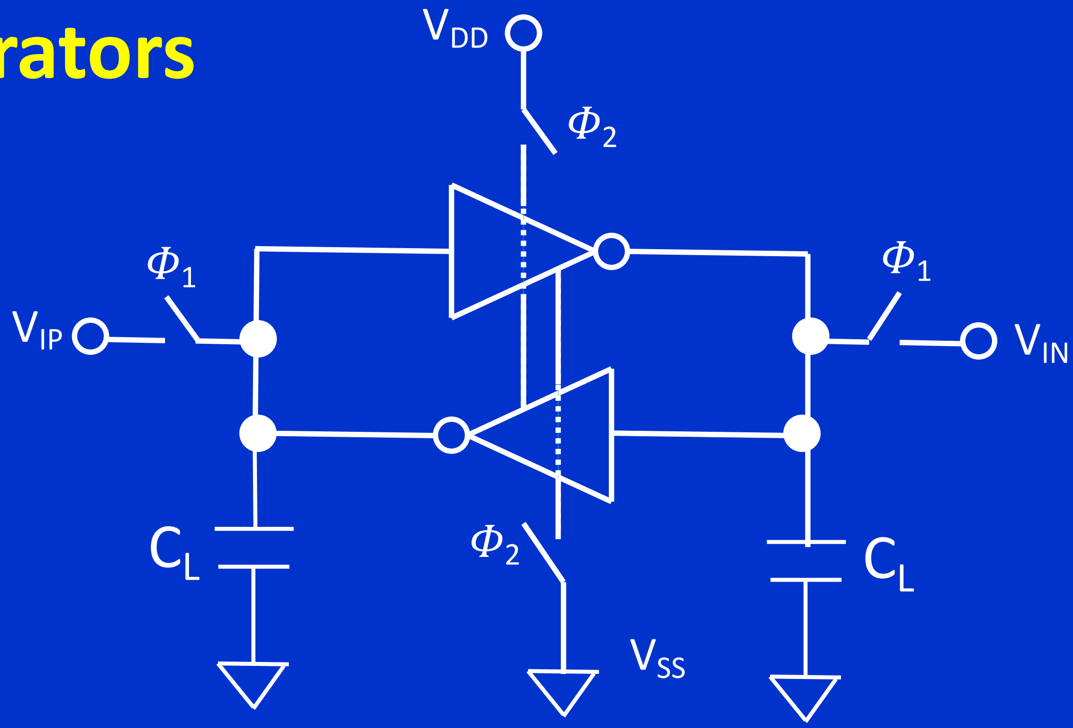
Module 12
Latch as a Comparator

References

- Prof. Boris Murmann's slides from "VLSI Data Conversion Circuits", Stanford University, 2013.
- Section "Latched Comparators" onwards from chapter "Comparators", Analog Integrated Circuit Design by T. C. Carusone, D. A. Johns and K. Martin, J. Wiley & Sons, 2012.
- "Clocked Comparator" from chapter "Submicron CMOS Circuit Design", CMOS Mixed-signal Circuit Design by R. Jacob Baker, Wiley India, IEEE press, reprint 2009.
- "Comparator" from chapter "Nonlinear Analog Circuits", CMOS Circuit Design, Layout and Simulation by R. Jacob Baker, Wiley India, IEEE press, 2008.
- "The StrongArm Latch", B. Razavi, IEEE Solid-State Circuits Magazine, Spring 2015.

Replacing Cascade of N Integrators with a Closed Loop of Integrators

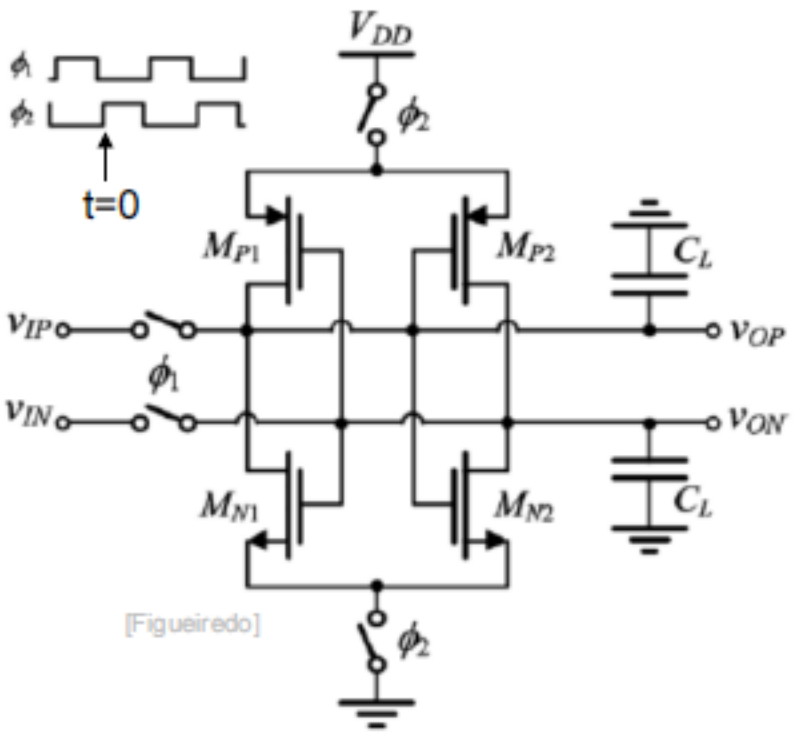
Latch (regenerative sense amplifier)



- Each inverter is a G_m module driving a capacitive load and hence behaves as an integrator.
- A closed loop of two inverters is mimicking cascade of infinite number of integrators.

Latch as a Comparator

Conceptual Circuit



ϕ1: Set up initial condition (v_{OD0})
ϕ2: Enable positive feedback

$G_m = g_{mN} + g_{mP}$ Inverter Transconductance

$$\frac{dv_{OP}}{dt} = \frac{i_1(t)}{C_L} = -\frac{G_m v_{ON}(t)}{C_L}$$

$$\frac{dv_{ON}}{dt} = \frac{i_2(t)}{C_L} = -\frac{G_m v_{OP}(t)}{C_L}$$

$$\tau = \frac{C_L}{G_m}$$

$$v_{OD}(t) = v_{OP}(t) - v_{ON}(t)$$

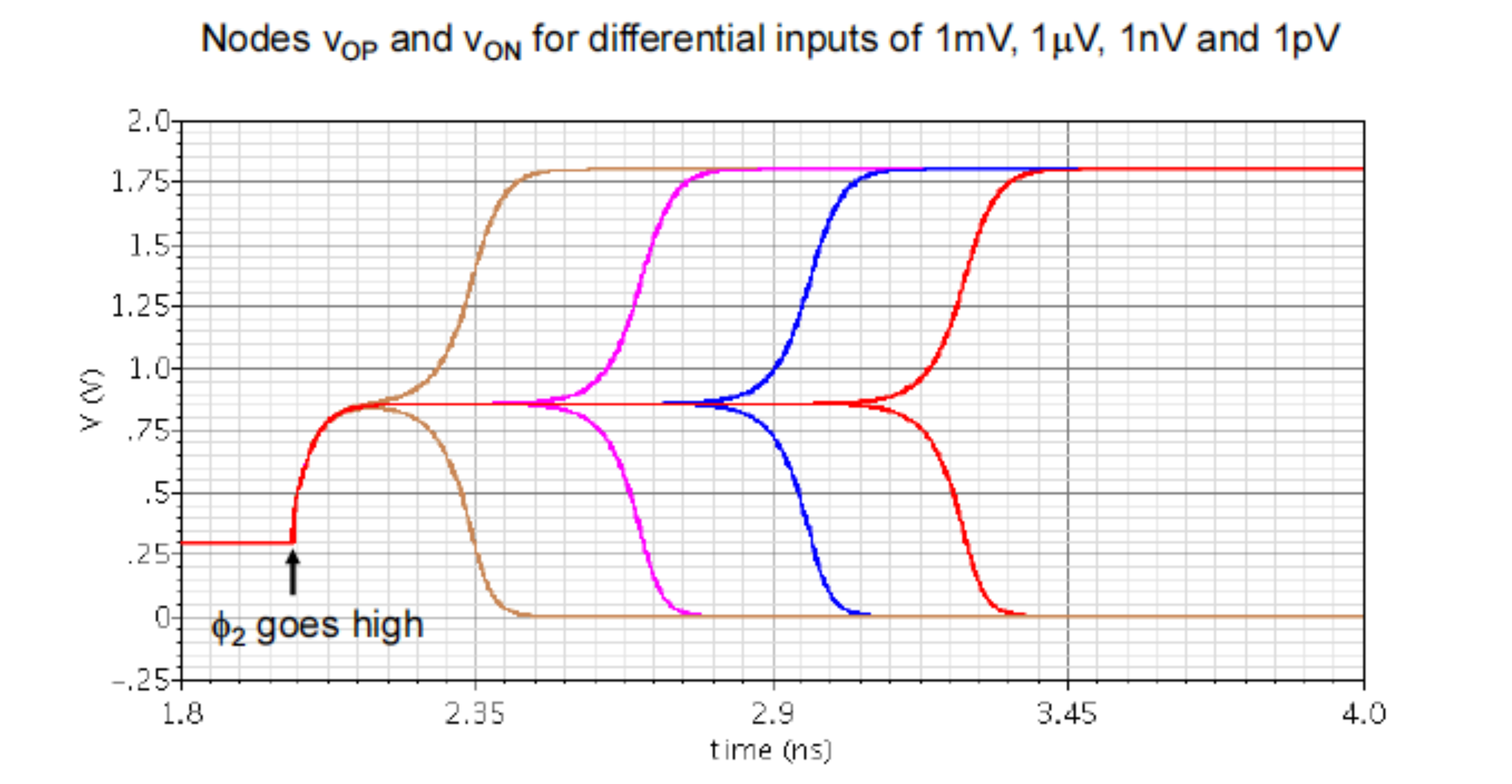
$$v_{OD}(t) = v_{OD0} \cdot e^{t/\tau}$$

$$A(t) = \frac{v_{OD}(t)}{v_{OD0}} = e^{t/\tau}$$

Latch gain

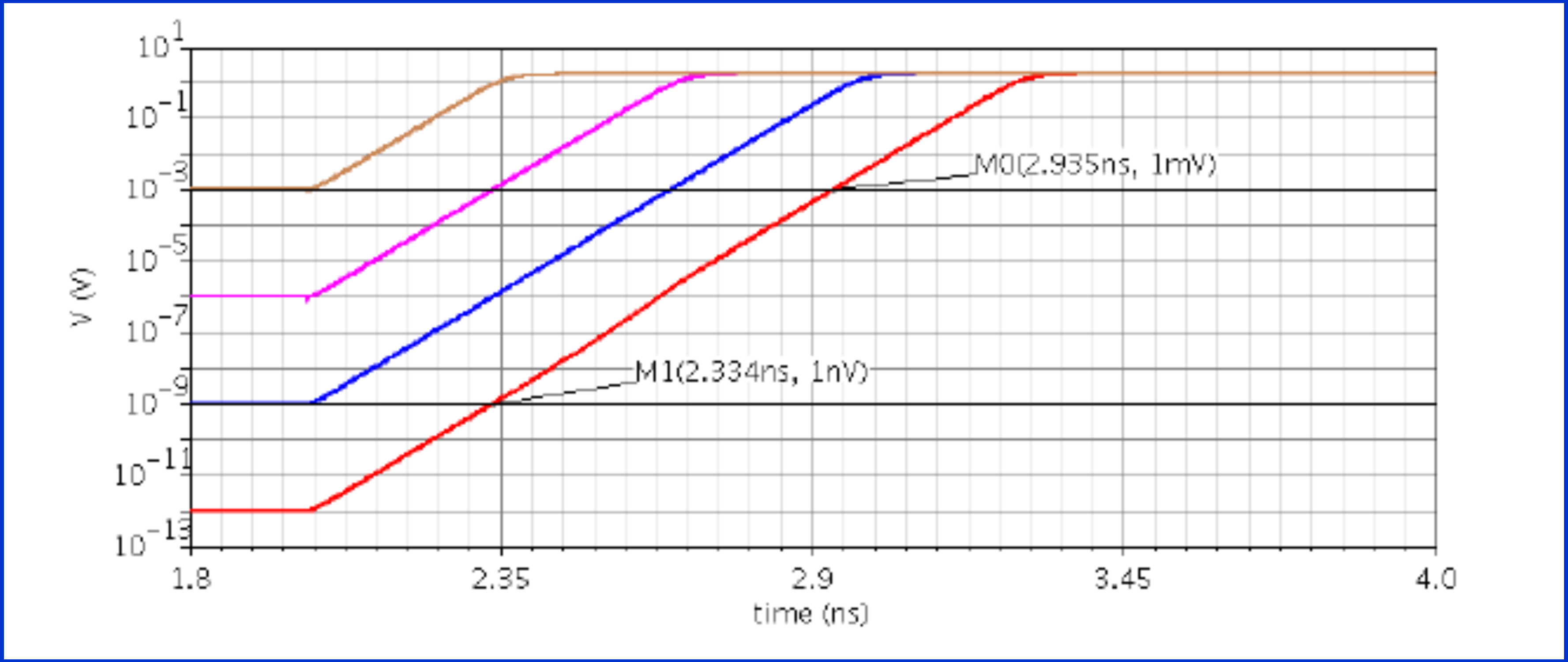
B. Murmann's course, Stanford Univ., 2013

Latch as a Comparator - Example



B. Murmann's course, Stanford Univ., 2013

Linear Behavior of log(V_{diff}(t)) versus t and Initial Condition



B. Murmann's course, Stanford Univ., 2013

Analysis of Latch Delay

$T_{d,latch} = \tau_{latch} \ln\left(\frac{v_{od\,logic}}{v_{od\,0}}\right)$

$C \approx a \times WLC_{ox}$, $1<a<2$

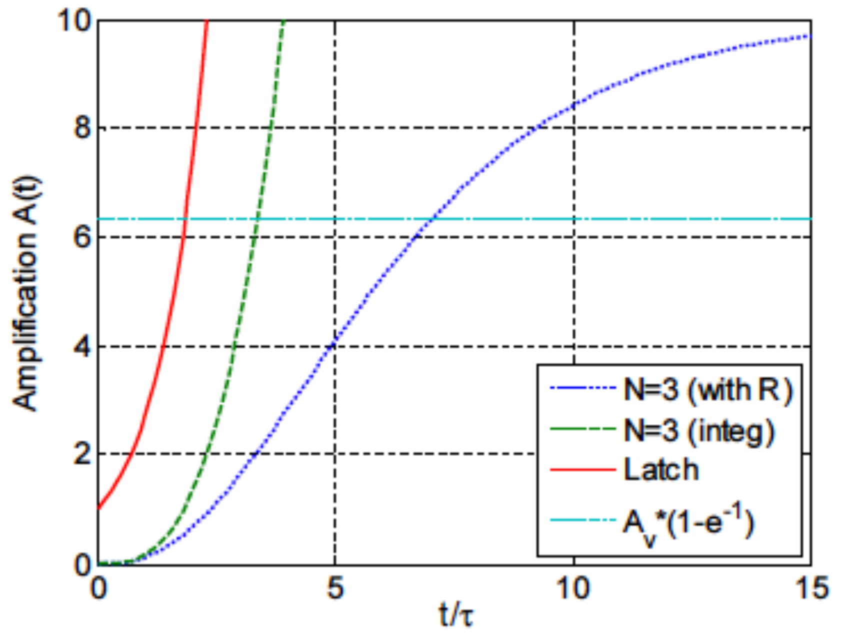
$g_m \approx b \times \mu C_{ox}\, W/L \times V_{GST}$, $0.5<b<1$

(either NMOS or PMOS transistor) $\Rightarrow \tau_{latch} \approx d \times L^2/(\mu_n \times V_{GST})$

where $1<d<4$

Velocity saturation:

$\tau_{latch} \approx a \times L/v_{sat}$



- K. Martin's book, 2012
- B. Murmann's course, Stanford Univ., 2013

End of Lecture 11